Preliminary Program of the ASIS 2009

October 20, 2009

12:00-13:45 *Registration of participants in Muzeum umění (Museum of Fine Art)*

13:45-15:00 *Session*

BREJCHA Milan, EVIDA Plzeň: Modelové vidění

KVASNICA Peter – PÁLENÍK Tomáš, TUAD Trenčín: Simulation in Flight Simulator with the Hybrid Distributed-Shared Memory Architecture

BOGDAN Lucyna – PETRICZEK Grażyna, PAN Warszawa: Modeling of a sewerage system

19:30-21:00 Registration of participants in Best Hotel Garni, Cap of Vine

October 21, 2009

09:00-10:00 *Registration of participants in Muzeum umění (Museum of Fine Art)*

10:00-12:00 *Session*

GLADYSZ Jakub – WALKOWIAK Krzysztof, WUT Wrocław: Analysis of Cut Inequalities for the Uncapacitated Network Design Problem with Simultaneous Unicast and Anycast Flows.

GRZYBOWSKI Arkadiusz, WUT Wrocław: Reliability of MPLS networks

KOLÁŘ Dušan, FIT VUT Brno: Exploitation of Scattered Context Grammars to Model Constraints between Components

ROZMAN Jaroslav, FIT VUT Brno: 2D and 3D Motion Model with Uncertainty

HALKO Jozef – MAŠČENIK Jozef: TU Košice v Prešove: Simulation the Newly Developed Multiple-Output Gearbox

12:00-13:30 *Diner Break*

13:30-17:00 *Session*

OLIINYK Oksana – WOZNIAK Michal, WUT Wrocław: Risk in IT projects and its influences on their successes.

RYBA Przemysław – KASPRZAK Andrzej, WUT Wrocław: Minimal Cost Allocation of Computing Resources in Two-Tier Hierarchical Wide Area Networks.

KŘOUSTEK Jakub, FIT VUT Brno: Usage of Decompilation in Processor Architecture Modeling

KŘIVKA Zbyněk – JIRÁK Ota, FIT VUT Brno: Simulation-based Debugging of 8-bit Softcore Processor

PENIAK Peter – KÁLLAY Fedor, ŽU Žilina: Komponentový model pri riešení komplexnej systémovej integrácie priemyselných systémov

MARKOWSKI Marcin – KASPRZAK Andrzej, WUT Wrocław: Computational properties of servers' allocation algorithms for Wide Area Networks

LYSIAK Rafal – KOSZALKA Leszek – POZNIAK-KOSZALKA Iwona, WUT Wrocław: Simulation-Based Evaluation of MBF Task Allocation Algorithm in Mesh-Connected Processors

CHODACKI Miroslaw – GOSCINIAK Ireneusz, SU Sosnowiec: Built-In Self-Test Evolutionary Design

18:30-21:30 *Social Evening in Vinotéka*

October 22, 2009

09:30-12:30 *Session and Final Session*

IVANOVS Mihails, TU Riga: The Application of Generative Programming in the Development of Electronic Commerce Systems

KLINK Janusz, WUT Wrocław: Simulation of Network Impairments and their Influence on VoIP QoS

BACHRATÝ Hynek, ŽU Žilina – KRŠÁK Emil, ŽU Žilina – ŠOTEK Karel, UP Pardubice: Bitové kalendáře v konstrukci jízdních řádů

ZMYSLONY Marcin – WOZNIAK Michal, WUT Wrocław: Influence of fusion methods on quality of classification

ĎUĎÁK Juraj – ČIČÁK Pavel, TUAD Trenčín: Model protokolu Modbus pomocou farbených Petriho sietí

ŠMERINGAIOVÁ Anna, TU Košice: Dynamické skúšky ozubených prevodov

MAŠČENIK Jozef – NOVÁKOVÁ Martina – HAĽKO Jozef, TU Košice: Návrh a simulácia skúšobného stendu na rotačné tvárnenie tenkých plechov