

**General Chair**

*Bernd Straube*  
 Fraunhofer IIS/EAS Dresden, D  
 straube@eas.iis.fhg.de

**General Vice-Chair**

*Zdeněk Kotásek*  
 Brno University of Technology, CZ  
 kotasek@fit.vutbr.cz

**Program Chair**

*Erik Jan Marinissen*  
 Philips Research Eindhoven, NL  
 erik.jan.marinissen@philips.com

**Program Vice-Chair**

*Ondřej Novák*  
 Technical University of Liberec, CZ  
 ondrej.novak@vslib.cz

**Organising Committee Chair**

*Richard Růžička*  
 Brno University of Technology, CZ  
 ruzicka@fit.vutbr.cz

**Program Committee**

E. Aas (Norway), V. Castro Alves (Brazil),  
 M. Balakrishnan (India), S. Demidenko  
 (New Zealand), B. Dervisoglu (USA),  
 M. Engels (Belgium), J. Figueras (Spain),  
 N. Frištacký (Slovakia), E. Gramatová  
 (Slovakia), S. Hellebrand (Austria),  
 J. Hlavička (Czech Republic),  
 A. Hlawiczka (Poland), E. Hryniewicz  
 (Poland), L. Jozwiak (The Netherlands),  
 Z. Kotásek (Czech Republic),  
 A. Krasniewski (Poland), K. Kuchcinski  
 (Sweden), H. Manhaeve (Belgium),  
 E.J. Marinissen (The Netherlands),  
 F. Novak (Slovenia), O. Novák (Czech  
 Republic), A. Pataricza (Hungary),  
 A. Pawlak (Poland), Z. Peng (Sweden),  
 I. Phillips (UK), P. Prinetto (Italy),  
 M. Renovell (France), B. Rouzeyre  
 (France), J. Sosnowski (Poland),  
 A. Steininger (Austria), V. Stopjaková  
 (Slovakia), B. Straube (Germany),  
 J. Sziray (Hungary), J.-P. Teixeira  
 (Portugal), R. Ubar (Estonia), K. Vlček  
 (Czech Republic), C.-W. Wu (Taiwan),  
 H.-J. Wunderlich (Germany), V. Yarmolik  
 (Belarus), Y. Zorian (USA)

**Organising Committee**

L. Sekanina, J. Strnadel, M. Linhart,  
 R. Čejka (Czech Republic)

**Steering Committee**

J. Hlavička - chair (Czech Republic),  
 D. Badura (Poland), N. Frištacký  
 (Slovakia), E. Gramatová (Slovakia),  
 A. Hlawiczka (Poland), E. Hryniewicz  
 (Poland), Z. Kotásek (Czech Republic),  
 A. Krasniewski (Poland), H. Manhaeve  
 (Belgium), O. Novák (Czech Republic),  
 A. Pataricza (Hungary), A. Pawlak  
 (Poland), M. Renovell (France), B. Straube  
 (Germany), J. Sziray (Hungary), R. Ubar  
 (Estonia), K. Vlček (Czech Republic)



CALL FOR PAPERS



# IEEE DDECS 2002

5<sup>th</sup> IEEE International Workshop on  
 Design and Diagnostics of Electronic Circuits and Systems 2002



April 17-19, 2002  
 Brno, Czech Republic

**Sponsored by:**

- IEEE Computer Society Test Technology Technical Council
- Faculty of Information Technology,  
 Brno University of Technology, Brno, Czech Republic

**Topics include but are not limited to:**

- Novel architectures for SOC
- Modelling and simulation for SOC
- Virtual components and IP-based design
- Web-based collaborative engineering
- New trends in ASIC/FPGA design
- Hardware-software co-design
- Formal methods in system design
- Bio-inspired hardware
- Testability issues: DFT, BIST, BOST, test reuse
- Defect-oriented/specification-oriented testing
- On-line testing and safety
- Analogue and mixed signal circuit testing
- Alternative test methodologies: IDDQ/IDDT/delay
- Test and design quality and economics

**Submission of Papers**

The working language of the workshop is **English**. Prospective authors are invited to submit full papers that should not exceed 8 pages. Electronic submission through the workshop's web page in PostScript or PDF format is required. Please identify the contact author with his/her complete mailing address, phone number, fax number, and e-mail address.

**Industrial Experiences**

DDECS 2002 especially encourages the submission of presentation proposals on industrial experiences. The submission of an extended abstract suffices, although full papers are of course also welcomed.

**Paper Acceptance**

Each accepted paper has to be presented by one of the authors at the workshop and must be accompanied with the registration fee.

**Author's Schedule**

Deadline for submission	January 20, 2002
Notification of acceptance	February 24, 2002
Deadline for submission of final manuscripts	March 17, 2002

More information can be found on <http://www.fit.vutbr.cz/events/ddecs02>