Saving network traffic to dynamic memory

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The most common operations performed by network elements are scheduling and switching of packets in queues. At each input interface, each packet is stored in an input buffer. Based on the information contained in the packet, output interface where the packet is switched is chosen. The output interface then performs packet scheduling. Scheduling algorithms compute departure time of each packet according to the characteristics of the transmitted traffic. Algorithms for scheduling often use multiple queues. They select a queue to which a packet is stored and a queue from which is a packet sent to the network.

With the increasing demands for the network speed, demands for the speed of algorithms and memory used for queues and buffers are also increasing. Acceleration of scheduling and switching algorithms can be achieved by implementing in hardware (e.g. FPGA). Enough memory needed for a queue provides a dynamic memory (DDR SDRAM).

The limiting factor for dynamic memory is a speed of data reading and writing. The memory reaches a top speed for burst transfers. For writing to the memory in burst mode it is necessary to have a buffer before the dynamic memory in which are burst data prepared. For similar reasons it is necessary to have a buffer for the read data. On the size of the buffer is depending the maximum size of the burst transfer and hence the speed of data transmission. Because the price of these buffers is high and FPGAs have only a very limited size of these buffers, it is desirable to minimize the size of these buffers.

Using a model described by Petri nets, the behaviour depending on the type of network traffic can be simulated. Based on an analysis of this model and based on tests with it, it is possible to design the optimal management and the size of the buffers.