IMPROVING TESTABILITY PARAMETERS OF PIPELINED CIRCUITS THROUGH THE IDENTIFICATION OF TESTABLE CORES

Zdeněk Kotásek Tomáš Pečenka, Josef Strnadel
Brno University of Technology
Faculty of Information Technology, Department of Computer Systems
Božetěchova 2, 612 66 Brno, Czech Republic
phone: +420 5 4114 1223, fax: +420 5 4114 1270
e-mail: kotasek,pecenka,strnadel@fit.vutbr.cz

Abstract. *A new methodology of selecting registers into scan chain is presented. It is based on the identification of testable cores. The methodology is supposed to be used preferably for pipelined circuits consisting of a high number of stages. In the paper, the idea of testable cores is illustrated and defined. The method based on a genetic algorithm is described and verified on several typical pipelined circuits. Experimental results are discussed and summarized in the table. At the end of the paper, conclusions and future research perspectives are indicated.*

1 Introduction

In some applications, high performance of a resulting circuit design (typically a high-end microprocessor, communication or multimedia circuitry) is demanded. As the maximum clock rate of a circuit is determined by a maximum register-to-register delay, the maximum delay can be then reduced through additional registers included into circuit structure. Such a technique is referred to as *pipelining* and a circuit designed using this technique is called a *pipelined circuit*. Also, it is known fact that besides the demanded functionality, good diagnostics properties of resulting circuit are required. This paper does not deal with an approach to an efficient design of a particular application-specific pipelined circuit, but it presents a new method of improving testability of a general pipelined circuit design.

As a result of some design for testability methodologies a subset of registers is identified through which the test vectors will be applied and responses to them observed. It is supposed that the registers will be converted either to scan registers or BIST elements. Then, the problem of testability analysis can be then seen as the problem of the identification of components to be tested in the *CUA* (*Circuit Under Analysis*) and the identification of registers through which test sequences will be applied to components. Those, so-called *scan* methodologies for selection of registers into the scan chain have been widely published and described recently. They fall into two main groups: *full scan* and *partial scan*. In partial scan, flip-flops (FFs) are selected in such a way that the remainder

of the circuit has certain desirable testability properties. Existing approaches for selecting FFs for partial scan can be classified as *testability analysis based* [2], *test generation based* [14] and *structural analysis based* [11]. All of these techniques suggest testability modifications after the completion of the design and are incapable of suggesting behavioural modifications by identifying testability bottlenecks in the design behaviour during the design process. Some methods exist which are based on inserting test registers in order to obtain self-testable circuits [1], [24], several algorithms were developed to select partial scan FFs to break feedback cycles [8], [16]. Other methods exist for re-ordering of scan cells [12] to minimize power dissipation and consumption [7], reduce the area overhead [23], data volume [18] or test length [9], to achieve acceptable trade-offs [4, 6], to improve an attainability [21] of states etc. [10, 15, 17, 20]. In many cases, an optimization algorithm is exploited to find the acceptable (sub-optimal) solution.

One possibility how to identify the set of registers for the test application process is by means of exploration of whole search space of the problem. Those methods are based on exhaustive search: they simply visit all points in the search space in some order and retain the best solution visited. It is evident that such approaches can be used in structures in which the number of registers is not high. Other (i.e., optimization) methods only visit part of the search space because the number of points visited may grow exponentially (or worse) with the problem size. In our research activities related to this paper, we have concentrated on searching for an optimizing method of the identification of components to be tested in the CUA, which might possibly lead to the reduction of CUA test application time (the components are referred to as testable cores in the paper). The results of our research are presented in this paper. We suggest how a *genetic algorithm* (*GA*) can be utilized to identify a subset of registers through which the internal components of CUA will be tested.

The paper is organized as follows. First, the concept of testable cores is defined together with the conditions they must satisfy, they properties and with the principles of their identification. General principles of GAs are then mentioned together with the way in which they are applied in our methodology. Finally, experimental results are summarized and trends for future research are indicated.

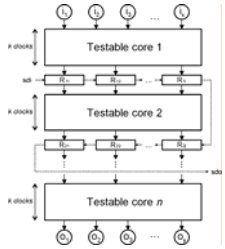
2 Problem Definition

The objectives of our research activities can be summarized as follows: definition of testable cores properties, development of GA-based methodology for the identification of testable cores and registers through which the test can be applied, implementation of the methodology, verification and evaluation of the methodology. As mentioned above, the identification of testable structures was one of the objectives of our research activities. A testable core is to be identified on the basis of the following definition:

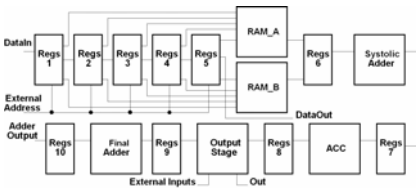
Definition 1: *Testable core* (*TC*) is a *register-transfer level* (*RT level, RTL*) structure, which satisfies the following conditions: (1) it is either separated from the rest of the circuit by registers, or it is directly connected to primary inputs/outputs (*PI*/*PO*s) – registers and *PI*/*PO*s are then denoted as *TC inputs/outputs* (*I*/*O*s), (2) it must be possible to test all internal components from the TC inputs/outputs (i. e. internal component *I*/*O*s must controllable/observable from/on TC *I*/*O*s), (3) no feedback loops are allowed to appear in the CUA, (4) none of registers inside the core is required to be scanned to guarantee testability of the core internal elements. The usual situation is such that there is more than one TC in the circuit. Then, the following additional conditions must be satisfied: (5) inner components of all TCs must be controlled by a very close number of clock pulses, (6) the

transportation of diagnostic data through the structure of all TCs requires equal (or very close) number of clock pulses to be generated, (7) no TCs structures are allowed to overlap.

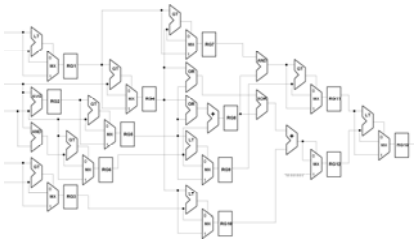
The principles of the methodology can be seen in Fig. 1a. TCs are separated from each other by registers, which are included into scan chain, as a result of testability analysis. Test vectors are applied and responses to them observed through registers. From the test application point of view, TCs are independent sub-circuits. The test of the CUA then consists of the test of TCs, which can be tested separately. The presumption for the test application is it can (hopefully) be scheduled in the way, which will allow apply test vectors and collect responses simultaneously for several TCs. Alike in the case of identification of registers for the scan, the identification of TCs is a problem, which can be solved in two ways – 1) through comprehensive structure analysis and searching for possible TCs (exhaustive search) or 2) through converting the problem into optimisation problem and reducing the search space. In our methodology, the problem of TCs identification is solved as the optimisation problem, GA is utilised for this purpose. As a result of applying the methodology, TCs are identified in the CUA together with registers, which separate them.



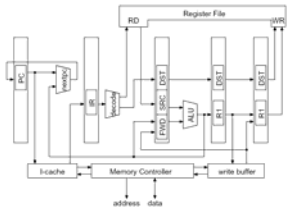
a) Testable cores–illustration



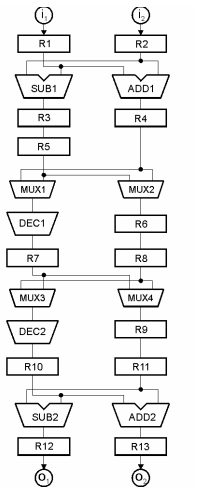
b) TITAC-2 processor architecture



c) FETX0 image filter



d) ARIES



e) mFFT circuit

Figure 1: Testable cores illustration example (a) and tested pipelined circuits (b–e)

3 Principles of Methodology Based on Utilizing Genetic Algorithm

Generally, to apply GA to a problem, it is necessary to identify: (1) meaningful representation for the candidate solutions; (2) a fitness function to assess different solutions; and (3) a set of useful genetic operators, that can efficiently select, recombine and mutate candidate solutions. All GAs require guidance to dir evolution towards better areas of the search space. They receive their guidance by *evaluating* every solution in the *population* (a set of so-called chromosomes, each of them represents certain element from the search space), to determine its *fitness*. The fitness of a solution is a score based on how well the solution fulfils the problem solution objective, calculated by a *fitness function*. GA operates with two populations – the *population of parents* and *population of offspring.* Over these populations so-called *reproduction process* (using genetic operators of *selection*, *crossover*, *mutation*) is performed until an individual with acceptable properties (i.e., with high fitness value) is found or until (during certain time) an individual with better than up to now found properties is found.

In our methodology, the chromosome represents the CUA subdivided into TCs and the fitness value reflects the quality of the individual (solution), the criteria being (1) how TCs satisfy conditions according to definition 1 and additional conditions, (2) testability parameters of the subdivided CUA. The problem of identification of TCs in a circuit (with n registers in its structure) can be simply transformed to a problem of identification of registers that separate these cores. The last mentioned problem could be encoded using a binary string (chromosome) of length

$$w = n \cdot \left(\lfloor \log_2 (k-1) \rfloor + 1 \right), \text{ where } k=2.(n+1) \quad (1)$$

Proposed fitness function returns a fitness value f that lies in <0, 1000> range and it pays that higher value is assigned to a chromosome that meets the requirements better; it consists of following partial values: $f_1 \in$ <0-550> value, evaluating the quality of circuit structure fragmentation to cores., $f_2 \in$ <0-250> value, evaluating the testability of a circuit fragmented into cores, $f_3 \in$ <0-200> value, evaluating the easiness of data transport through selected cores. The resulting fitness value f is defined as the arithmetic sum of f_1, f_2 and f_3.

4 Experimental Results

Proposed method for improving testability of pipelined circuits was verified on circuits (each of them represents a certain big group of pipelined circuits) **TITAC-2** [25] (Fig. 1b, it is a 32-bit microprocessor), **FETX0** (Fig. 1c, it is a digital circuit [19] designed for filtering bitmap images – it is used as a „salt and pepper noise filter"), **ARIES** [3] (it is a basic building block for the construction of convolutional filtering circuits, its simplified schema is depicted in Fig. 1d), **mFFT** [5] (Fig. 1e, it is a part of a pipelined digital circuit used for 4-point fourier transform computation). At the end of this section, the results gained are summarized in Tab. 1 and general evaluation of the applicability of our method to pipelined circuits is provided. Experimental results gained for circuits listed above are quantified in Tab. 1. The columns of the table are sectioned in three parts: fist part (**Quantified Parameter**) contains a name of a quantified parameter, second one (**Original Structure**) contains results for original structures of tested circuits and the last one (**Testable Core Implementation**) contains results for tested circuit after implementation of TCs by the method proposed in the paper.

On the basis of experiments with our method, following general conclusions can be done: (1) pipelined circuits are characterized by a very high level of testability (controllability, observability of inner nodes) in general, (2) proposed method is able to reduce a test length for given pipelined circuit, but it was observed that the fault coverage does not increase very much by its application in general. In certain cases, better results (i.e., with a higher fault coverage, but usually with the longer test length) can be achieved by other partial-scan based methods than using the proposed one method, (3) proposed method is especially applicable to purely pipelined circuits (i.e., circuits that do not contain any circuitry that can partially or fully flush or restart the pipeline) – e.g., mFFT or ARIES type, but it is not feasible for improving testability of the non-pure pipelined circuits (e.g. TITAC-2) and (4) the more pipeline stages a circuit structure consists of, the more efficient (higher test shortage) results can be expected by using our method.

5 Conclusions and Perspectives of Future Research

In our research we deal with the testability analysis of RT level circuits. In this paper, a new methodology based on the idea of testable cores is presented which can be used mainly for

pipelined structures. Although this idea is not new (see [13]), we suggest how this idea can be utilised for pipelined structures together with new principles of "how to identify testable cores in complex structures". We defined the requirements that must be satisfied by testable cores (i. e. features according to which testable cores are identified).

The identification of testable cores enables test application time to be reduced. It is due to the possibility of applying test in parallel both to testable cores and to internal components of testable cores and effective utilisation of scan chains. Another advantage of the methodology can be seen in the fact that the problem of testability of CUA as a whole has been subdivided into partial problems of testability cores testability. On the other hand, as a negative factor we see that the number of registers, which need to be included into the scan chain can increase. Moreover, the analysis of CUA structure resulting in the identification of testable cores can be rather complicated procedure.

Table 1: Summarized experimental results.

Quantified Parameter	**Original Structure**				**Testable Core Implementation**			
	TITAC-2	mFFT	FETX0	Aries	TITAC-2	mFFT	FETX0	Aries
Total number of PI/PO	134/38	21/16	7/1	32/24	140/43	24/18	10/3	34/25
No. PI/PO for test purposes	-	-	-	-	6/5	3/2	3/2	2/1
Total number of nodes	7921	510	947	1547	8192	515	957	1553
No./% of controllable nodes	3281/ 41.4%	494/ 96.9%	939/ 99.2%	1545/ 99.9%	5412/ 66.0%	499/ 96.9%	949/ 99.2%	1550/ 99.6%
No./% of observable nodes	2560/ 32.3%	502/ 98.4%	924/ 97.6%	1541/ 99.6%	4850/ 59.2%	507/ 98.4%	937/ 97.9%	1540/ 99.1%
Average testability	0.268	0.859	0.842	0.576	0.563	0.878	0.854	0.808
Gate overhead	-	-	-	-	1.0%	4.4%	3.0%	1.0%
Estimated test length	180540	18688	13822	56510	176320	18628	12962	49526
Estimated test contraction	-	-	-	-	2.3%	3.2 %	6.6%	12.4%

In the future, the methodology of testable cores can be further directed into the following areas: the implementation of the methodology in the formal environment introduced in [2] with which the identification of testable cores based on analytical approaches is combined, an automated design of test controller in the way which will allow to apply test in parallel both to testable cores and to internal components of testable cores, the considerations on the possibility of utilising the set of test responses of one testable core as the subset of test patterns for another testable core which can further reduce the test application time, the organisation of scan registers into scan chains.

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