METHODOLOGY OF SELECTING SCAN-BASED TESTABILITY IMPROVING TECHNIQUE

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Abstract. *In the paper, the solution of the problem of selecting the most optimal design-for-testability technique for register-transfer level digital circuits is demonstrated. A decision-making process that is able to solve the problem over a set of scan-based techniques is presented in the paper. The process decides among following testability improving techniques: identification of testable cores, covering of feedback loops by minimum set of scan registers, selection of registers into scan chains to achieve high level of parallelism during the test application.*

1 Introduction

An RTL component consists of registers, functional units and multiplexers. The registers represent the sequential part of the circuit and carry the state of the circuit while the combinational part includes functional units and multiplexers. Moreover, registers are seen as the elements through which the test to an RTL component as a whole can be applied and thus they become very important for the process referred to as testability analysis.

When it is stated that an element is transparent, then it means that data can be transported from its input to its output without being modified. It is evident that connections in a circuit are seen as transparent. The transparency property of elements in an RTL component is not guaranteed, unless the elements can operate in the operation mode denoted as i-mode [1].

During the testability analysis it can be discovered that the structure of the component does not allow the test to be applied to some internal elements. In that case, a methodology which increases testability parameters must be used. From among them, scan methods can be mentioned. On the other hand, the methods based on the identification of feedback loops or testable cores can be mentioned as the methods for which the analysis of the circuit structure is done [4], [5].

The methodology for the identification of testable cores is based on partial scan approach. The methodology is based on the identification of testable cores fulfilling predetermined conditions of testable design. The cores are separated from each other by registers included into scan chains. The scan registers serve for testable cores as primary inputs/outputs [2].

To select registers to be included into scan chain, different criteria can be used – power consumption [7], [8], [11], [12], short test application time [3],[9],[10],[13], high fault coverage [6] or chip area overhead [8].

2 Motivation for Research

The goal of our research was to develop and implement algorithms for the selection of appropriate test application methodology for RTL structures. In the circuit structure, we try to recognize features which are typical for the selection of the particular test application methodology. The basic features are as follows: the existence of feedback loops, the existence of pipeline structures and the identification of elements which can be tested in parallel.

If the circuit contains feedback loops, then substantial reduction of the test application time can be achieved by eliminating the loops. If the circuit consists of testable cores, then a special methodology developed for this purpose can be used [2]. To apply the test in parallel, then it must be checked whether disjoint testing resources can be used for the test of functional units.

Some circuits have features which satisfy more than one test application methodology. Then, it can be concluded to use different test application methodologies for different parts of the circuit.

3 Principles of the Methodology

The principles of the methodology are based on the analysis of circuit structure and recognizing design aspects which are typical for RTL circuits. The identification of feedback loops is based on the detection of i-path in the direction from module output to module input. If such an i-path exists, then the module is seen as the module in a feedback loop. The algorithm passing through all i-paths between pairs of nodes within the circuit structure is as follows:

1. Starting element of an i-path is identified and recorded.
2. Direct successors of the last-inserted element are found. If there are two or more successors found, then the record for the starting element is duplicated.
3. The records having the last inserted element different from the starting element continue in execution of point 2. Other records represent the structure of feedback-loops. If there is no way to continue, the algorithm ends.

The second principle which is utilized by the methodology is that one of covering feedback loops by scan registers. The goal of the method is to cover the maximum number of feedback loops by the minimum set of scan registers. The algorithm of the method is as follows:

1. On the basis of the information about detected feedback loops, a list of all loops containing at least one register is created.
2. If a loop exists which is covered by only one register (i.e. the register is indispensable to cover the loop) then the register has to be included into scan and loops covered by the register are removed from the list.
3. It is evaluated how many feedback loops are covered by the remaining registers. The register which covers the highest number of loops is inserted to scan and the loops covered by the register are removed from the list.

4. Algorithm is finished when there is no loop in the list to be covered.

Even when all feedback loops are covered by scan registers, it may happen that not all modules will be testable through the registers included into the scan chain. Thus, it is necessary to check which extra registers should be inserted into scan in order to be able to test the maximum number of in-circuit modules by means of scan. The principles of the analysis are as follows:

1. First, it is analyzed which in-circuit modules can be tested through the registers included into scan chain.
2. The list of nodes which must be controlled and the list containing the nodes which must be observed are created.
3. The register that covers the highest number of elements in both of the lists is included into the scan. The elements covered by the register are removed from the lists.
4. Algorithm ends when it is not possible to cover any element in the list.

If there are no feedback loops in the (sub)circuit structure, the structure can be referred to as the pipelined structure. Test application time for such structures can be reduced if parallel testing of circuit parts is possible. The sub-circuits which can be tested in parallel are called testable cores. They satisfy predetermined conditions of testable design and are separated from each other by registers included into scan chains. The scan registers serve for testable cores as primary inputs/outputs

The number of clock cycles needed to transport diagnostic data from the test input register to inputs of tested-module (within the testable core) must be the same as the number of clock cycles needed to transfer diagnostic data in the direction from tested module outputs to the test output register. Test input and test output registers of testable cores are then inserted into scan chains. The test cores which are tested in parallel within the same test-phase are tested by the same number of clock cycles. The principle of the test scheduling algorithm is as follows: the greatest set of testable cores each requiring the same number of clocks for testing purposes is found. From the set, the greatest resource-disjoint subsets are extracted and inserted into the same test phase. The process is repeated until a testable core exists that is not inserted in a test phase.

The scheme representing the principles of the methodology is given in Fig. 1.

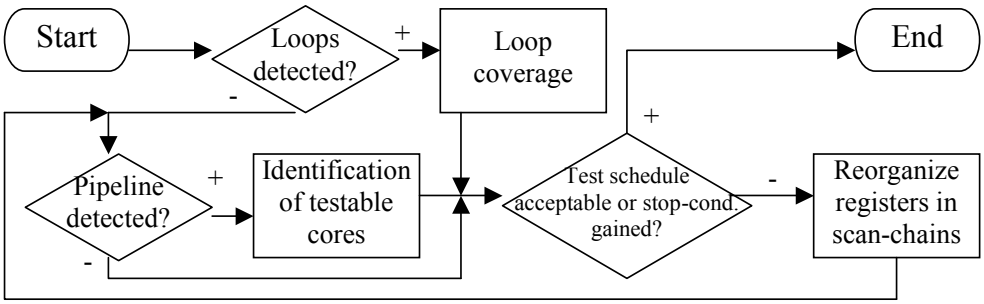

Figure 1: Flow-chart of the methodology

4 Conclusions and Perspectives for the Future

The methodology was verified on Bert, Diffeq, Paulin and Tseng benchmark circuits. For all circuits the following features were derived: 1) testability of original (and modified)

circuit structure, 2) the number of feedback loops within the original and modified circuit structure, 3) the need to include registers into scan chains and their number, 4) resulting number of test phases, 5) resulting number of testable cores.

As the main result of the research we see that the methodology allowing to analyse RTL structure was developed and implemented. The structure of the circuit is checked and feedback loops are eliminated, if there are any. Other aspects of the analysis which are taken into account are: the existence of pipeline structures (without feedback loops) and the possibilities of applying the test in parallel. The research in the future can be directed towards implementing other DfT techniques into the system together with developing criteria allowing to accept decisions on whether the particular technique is convenient for the RTL component being analyzed.

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