Evolution of Multifunctional Combinational Modules Controlled by the Power Supply Voltage

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Abstract

Polymorphic electronics provides a new way for obtaining circuits that are able to perform two or more functions depending on the environment in which they operate. These functions can be activated under certain conditions by changing control parameters of the circuit (such as temperature, power supply voltage, light etc.). Existing polymorphic gates are difficult to use as building blocks in complex digital circuits. In this paper, some modifications of existing polymorphic gates are proposed in order to utilize them in non-trivial digital multifunctional circuits. The presented multifunctional circuits composed of these gates represent the most complex multifunctional circuits available nowadays. In particular, NAND/NOR and AND/OR polymorphic gates controlled by the power supply voltage are discussed and used in circuits such as the five-bit majority/AND circuit and three-bit multiplier/six-bit sorting network circuit.

1. Introduction

Polymorphic electronics provides a new way for obtaining circuits that are able to perform two or more functions depending on the environment in which they operate. [9]. These functions can be activated under certain conditions by changing control parameters of the circuit (such as temperature, power supply voltage, light etc.).

In the recent years, several polymorphic gates have been discovered [9, 10]. For example, NAND/NOR gate controlled by the power supply voltage (Vdd) is available: This circuit operates as NAND when Vdd is 3.3V and as NOR when Vdd is 1.8V. Some of them have been fabricated and evaluated in a real environment [8]. In another research [6, 5, 1], multifunctional combinational modules composed of polymorphic gates were designed by means of evolutionary techniques. The resulting circuits are composed of standard as well as polymorphic gates and exhibit various unusual functions, for example, one of these circuits could operate as a two-bit adder when Vdd is 3.3V and as a two-bit multiplier when Vdd is 1.2V. However, it was assumed in these papers that polymorphic gates can be utilized as standard building blocks and that these gates are reliable and electrically fully functional.

This paper shows that the existing polymorphic gates are difficult to use as building blocks in more complicated circuits, particularly because they exhibit some problems with driving other circuits connected at their outputs. The objective of this research is to modify existing polymorphic gates in order to use them as standard building blocks for complex digital circuits. These "robust" polymorphic gates are then utilized in some combinational circuits to achieve a multifunctional behavior. This paper solely deals with polymorphic circuits controlled by Vdd. All the presented results were obtained using PSpice simulations.

2. Polymorphic Electronics

The concept of polymorphic electronics was proposed by Stoica, Zebulum and Keymeulen [9]. In fact, polymorphic circuits are multifunctional circuits. The change of their behavior comes from modifications in the characteristics of components (e.g. in the transistor's operation point) involved in the circuit in response to controls such as temperature, power supply voltage, light, etc. [10, 9].

Research papers indicate many areas in which polymorphic gates could be utilized. The following list provides some examples (see a thorough analysis in [9, 10]):

- The automatic control of power consumption when battery voltage decreases (a circuit realizes another function for lower battery voltage; however, its structure remains unchanged).
- Implementation of a hidden function, invisible to the user, which can be activated in a specific environment (e.g. watermarking at the hardware level).

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Table 1. Examples of existing polymorphic gates and their implementation cost (# of transistors)

Gate	Values	Control	Trans.	Ref.
AND/OR	27/125°C	temperature	6	[9]
AND/OR/XOR	3.3/0.0/1.5V	ext. voltage	10	[9]
AND/OR	3.3/0.0V	ext. voltage	6	[9]
AND/OR	1.2/3.3V	Vdd	8	[10]
NAND/NOR	3.3/1.8V	Vdd	6	[8]

- Intelligent sensors for biometrics, robotics, industrial measurement, etc.
- Reverse engineering protection.
- Implementation of low-cost adaptive systems that are able to adjust the behavior inherently.

The following subsections survey the existing polymorphic circuits. While Section 2.1 provides examples of genuine polymorphic gates, Section 2.2 shows examples of combinational modules constructed using polymorphic gates.

2.1. Polymorphic Gates

If polymorphic gates were available as building blocks we could develop polymorphic electronics. The main problem is their design: All the existing polymorphic gates were discovered by means of evolutionary design techniques. It seems that a human designer is not able to accomplish this task at all.

Table 1 gives examples of the polymorphic gates reported in literature. For instance, the NAND/NOR gate is the most famous example [8]. The circuit consists of six transistors and was fabricated in a 0.5-micron CMOS technology. The circuit is stable for $\pm 10\%$ variations of Vdd and for temperatures in the range of –20° to +200°C. Note that the common NAND and NOR gates cost 4 transistors, the XOR gate can be implemented using 10 transistors and 2 transistors are needed to create the inverter in the standard CMOS technology.

No circuits more complex than a single gate have been reported that are designed at the transistor level.

2.2. Multifunctional Combinational Modules

Considering polymorphic gates as building blocks offers an opportunity to design multifunctional digital modules at the gate level. Table 2 surveys multifunctional combination modules reported in [6, 5, 1, 7]. For example, using the polymorphic NAND/NOR gate and the standard AND gate it is possible to create a circuit which operates as a two-bit multiplier in one environment and as a two-bit adder in the second environment. Once the circuit is designed at the gate level (abstracting thus from the electric level), it does not matter whether this circuit is "reconfigured" by Vdd or a level of temperature or light.

Table 2. Examples of multifunctional combination modules and their implementation cost (# of gates). SN stands for Sorting Network and Mult stands for Multiplier

Circuit	Gates	Gates used
5b parity/majority	14	NAND/NOR, XOR/XOR
5b parity/majority	13	NAND/XOR, XOR/NOR
2b Mult/4b SN	23	NAND/NOR, AND/AND
2b Mult/4b SN	27	$(a \vee \overline{b})$/XOR, XOR/$(a \wedge \overline{b})$
2b Mult/2b Adder	20	NAND/NOR, OR/XOR
2b Mult/2b Adder	23	NAND/NOR, AND/AND
n-bit up/down SN	–	AND/OR, OR/AND

These circuits were designed by means of evolutionary design techniques. In some cases, the circuits contain hypothetical polymorphic gates; in other cases they are composed solely of physically existing polymorphic gates. Research results indicate that it is very difficult to discover circuit topologies for nontrivial polymorphic circuits and that human designer is not able to accomplish this task because no suitable conventional design method exists. It was shown that is it useful to combine polymorphic gates with conventional gates in order to obtain compact polymorphic circuits [6].

3. Transistor-Level Simulation of Polymorphic Circuits

This section reports the results obtained from PSpice simulations of polymorphic gates and multifunctional combinational modules. Firstly, the polymorphic gates taken from [9, 8] are discussed in Section 3.1. Then, new versions of these gates are proposed in order to use them as standard building blocks for digital circuits. Section 3.3 presents novel multifunctional combinational modules simulated at the transistor level. All the circuits are considered to be "controlled/reconfigured" by changes in Vdd.

3.1. Simulation of Polymorphic Gates

3.1.1 Existing NAND/NOR Gate

Figure 1a shows the polymorphic NAND/NOR gate controlled by Vdd taken from [8]. Unfortunately, the paper [8] does not contain the values of transistor parameters. Hence we utilized standard values for the corresponding technology in our model. This gate operates as NAND gate when Vdd = 3.3V and as NOR gate when Vdd = 1.8V. For the both values of Vdd, the circuit operates with the same levels of logic signals, i.e. log. 1 is ≈ 1.8V and log. 0 is ≈ 0V (see Fig. 1b–c). That is not useful for our purposes because it makes impossible to connect this gate to standard logic gates whose logic levels strongly follow the value of Vdd. Hence this gate has not been utilized.

3.1.2 Existing AND/OR Gate

Figure 2a shows the polymorphic AND/OR gate controlled by Vdd taken from [10]. This gate operates as AND gate when Vdd = 1.2V and as OR gate when Vdd = 3.3V. For our purposes, it is useful that levels of logic signals follow the changes in Vdd; i.e. when Vdd = 1.2 then log. 1 is ≈ 1.2V and when Vdd = 3.3V then log. 1 is ≈ 3.3V (see Fig. 2c–d). However, our experiments showed that this gate is not able to drive similar circuits when Vdd = 3.3V. Therefore, the gate cannot be used as a standard building block.

3.2. Improved NAND/NOR and AND/OR Gates

In order to prepare a gate which can be utilized as a building block for polymorphic combinational modules we have modified the AND/OR gate described in the previous section (see Fig. 2b). A standard inverter was connected to its output to strengthen the output voltage levels. Thus we have obtained NAND/NOR gate that operates as NAND when Vdd is 1.2V and as NOR when Vdd 3.3V. We carefully evaluated the gate and recognized that: (1) In contrast to the gate shown in Fig. 2a, the proposed gate is able to drive several similar gates (10 gates tested) because the inverter provides sufficient voltage/current levels. (2) This gate works up to a few MHz (also with a load). (3) Typical current consumption is approx. 10 pA; however, it is 1uA when the input logic combination is 1-0 and Vdd = 3.3V. (4) In contrast to the NAND/NOR gate from Figure 1a, the proposed gate can be connected to standard logic gates whose logic levels strongly follow the value of Vdd.

In order to make AND/OR gate, another inverter has to be connected to the proposed NAND/NOR gate. Although the AND/OR gate is composed of 12 transistors now, it is possible to use it in more complicated circuits (in contrast with the original AND/OR gate).

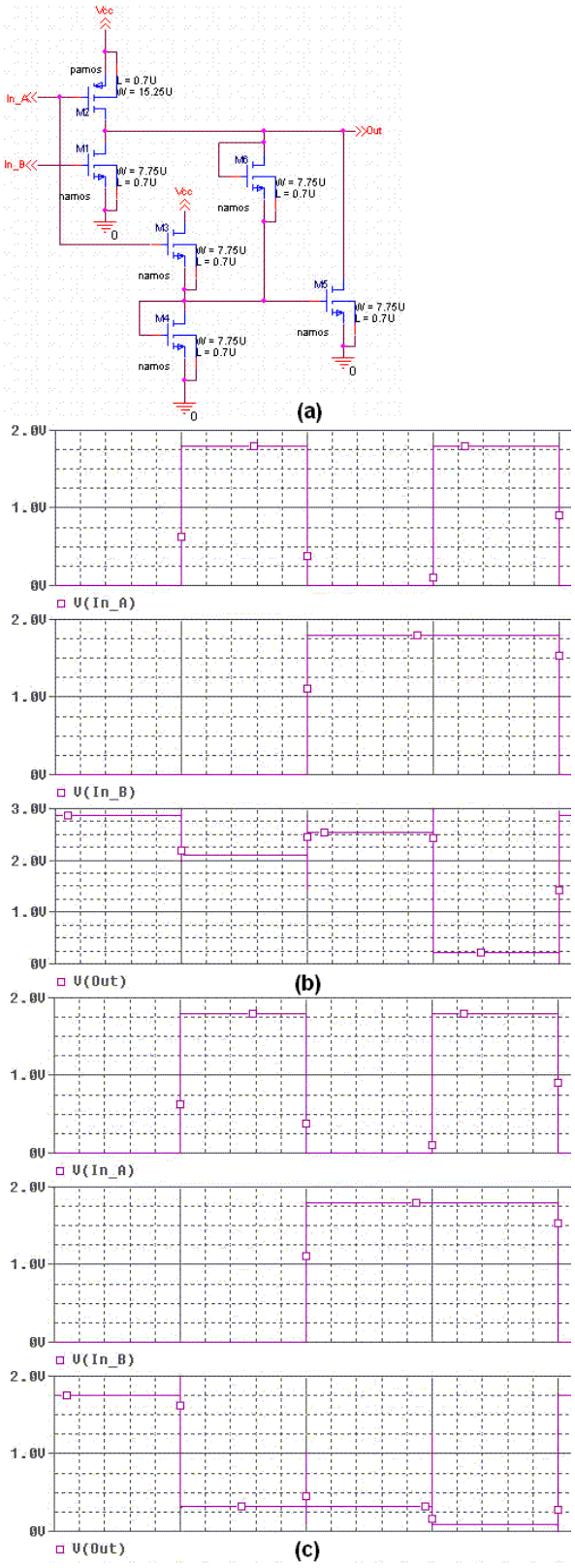

Figure 1. (a) NAND/NOR gate taken from [8], (b) NAND when Vdd = 3.3V, (c) NOR when Vdd = 1.8V

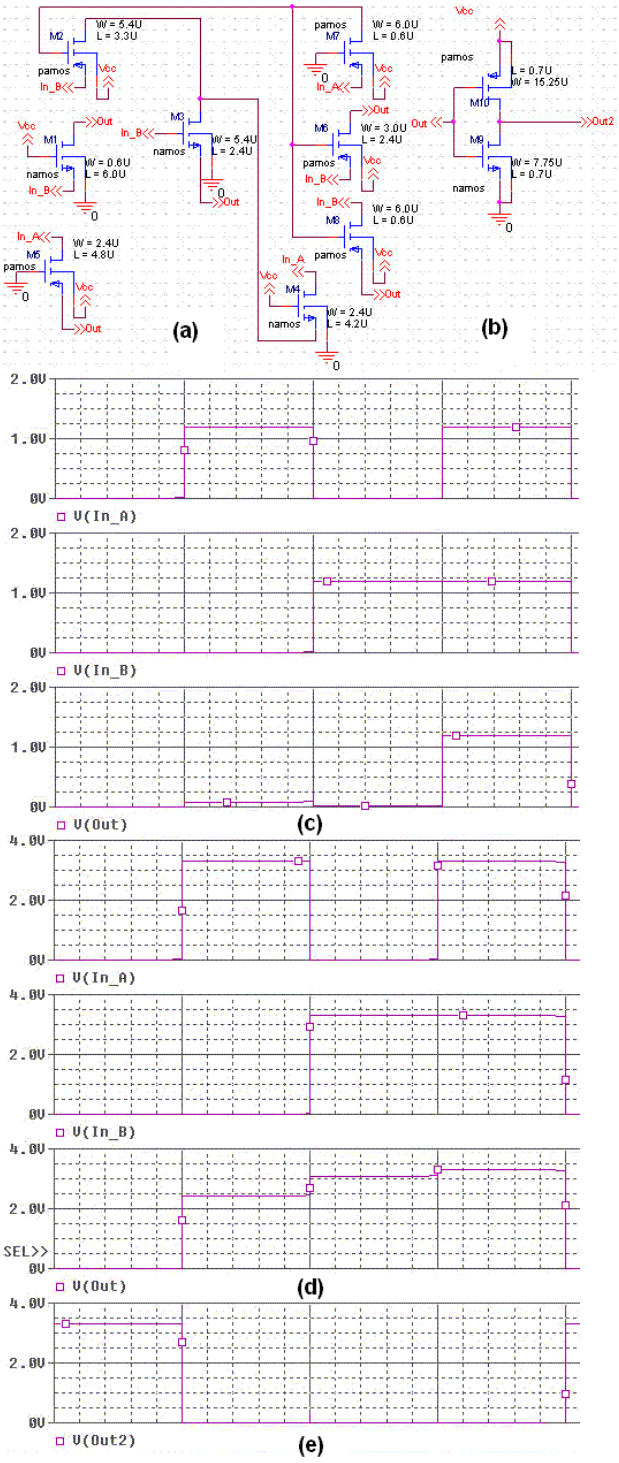

Figure 2. (a) AND/OR gate taken from [10], (b) an inverter connected, (c) AND for Vdd = 1.2V, (d) OR for Vdd = 3.3V, (e) NOR for Vdd = 3.3V when the inverter is considered

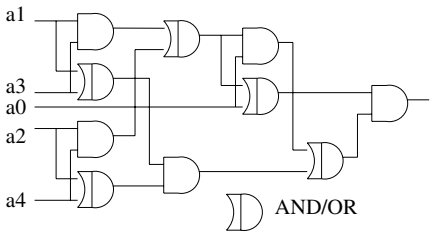

Figure 3. Five-bit majority/five-input AND circuit

3.3. Simulation of Multifunctional Combinational Circuits

From Table 2 it can be seen that when NAND/NOR and AND/OR polymorphic gates exist then the following polymorphic combinational modules can be implemented: five-bit parity/majority, five-bit boolean-symmetry/majority, two-bit multiplier/four-bit sorting network, two-bit multiplier/two-bit adder. Next subsections provide some examples. In particular, five-bit majority/five-input AND circuit and three-bit multiplier/six-input sorting network are proposed.

3.3.1 Five-bit Majority/Five-input AND

Figure 3 shows five-bit majority/five-input AND circuit which operates as follows:

- When Vdd = 3.3V then the circuit operates as a five-bit majority indicator, i.e. it returns log. 1 in case that three or more input signals are at log. 1; otherwise, it returns log. 0 (see Fig. 4b).
- When Vdd = 1.2V then the circuit operates as a five-input AND gate (see Fig. 4a).

The circuit consists of five standard AND gates and five polymorphic AND/OR gates. Its scheme was adopted from [4]. As a possible application we can imagine a system in which the logic conjunction of output values read from five components has to be indicated in case that Vdd = 3.3V (e.g. a full battery) to maintain a full functionality of the system. On the other hand, when a battery is running down (Vdd = 1.2V), the majority of the five is sufficient to switch the complete system to a low-power mode and to maintain a partial functionality.

3.3.2 Three-bit Multiplier/Six-input Sorting Network

In order to demonstrate transistor-level simulations of more complex multifunctional modules, Cartesian genetic programming [3] is utilized to evolve the three-bit

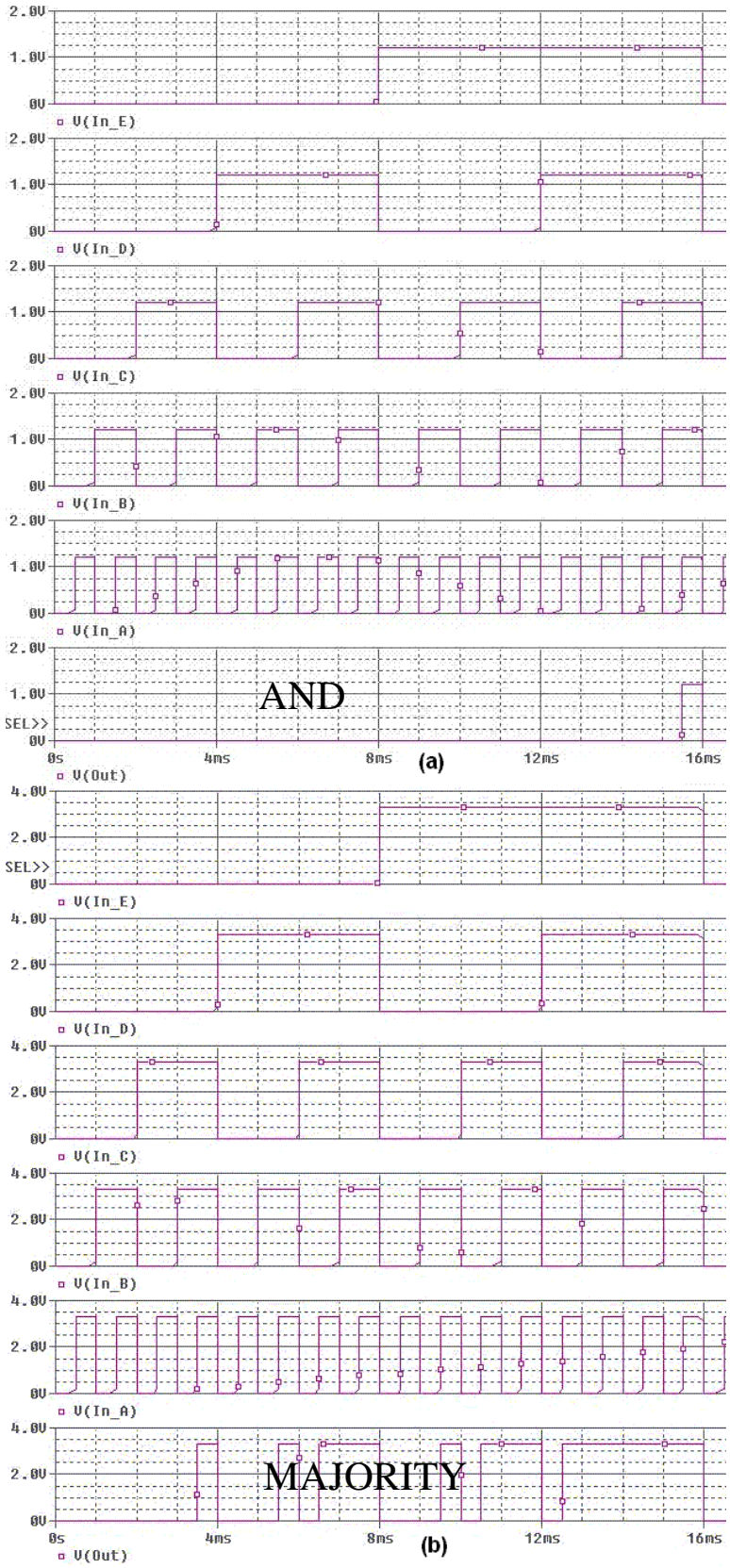

Figure 4. Simulation of 5bit majority/AND circuit: (a) AND for Vdd = 1.2V (b) majority for Vdd = 3.3V

multiplier/six-input sorting network at the gate level using the NAND/NOR polymorphic gates and some standard gates. According to the evolved gate-level scheme, a transistor level scheme was build using NAND/NOR gates controlled by Vdd (see Fig. 2b) and standard gates. The circuit operates as follows:

- When Vdd = 3.3V then the circuit operates as a six-input sorting network, i.e. it sorts the input bits (see Fig. 6b).
- When Vdd = 1.2V then the circuit operates as a three-bit multiplier (see Fig. 6a). Bits 0–2 are utilized for operand 1 and bits 3–5 for operand 2.

Cartesian genetic programming is utilized with the following parameters: Circuits were sought in an array of 120 x 1 two-input programmable elements. Each of them is able to perform one of the functions: (0) NAND/NOR, (1) AND, (2) OR, (3) XOR, (4) NAND, (5) NOR, (6) NOT a, (7) NOT b, (8) c = a, (9) c = b [identity]. The mutation operator modifies two randomly selected genes of the chromosome. Population size is 15. In fitness function, all possible input combinations are applied at the primary inputs of the circuit and the number of bits calculated correctly in both modes is considered as the fitness value. When a perfect functionality is obtained the number of gates is getting to minimize.

The best solution shown in Fig. 5 was discovered in the generation 10,244,650. It consists of 57 gates: 17 x NAND/NOR, 13 x AND, 6 x OR, 5 x XOR, 10 x NAND, 1x NOR, 1 x NOT a, 1 x c = b, 3 x c = b. Its functionality has not been optimized yet; however, it is easy to see that 4 programmable elements can be omitted as they operate as identity. Fig. 6 shows the simulation results in both modes. In order to fit this plot to a single page, only 8 input combinations are visible in Fig. 6 (The three lowest bits were set at log. 1. All possible input combinations are set only at the three highest bits.).

Note that the best known implementation of three-bit multiplier consists of 23 gates [11] and the best known implementation of six-input sorting network consists of 24 gates (AND and OR) [2]. From this point of view it seems that the evolved circuit is not optimal (53 gates are utilized) and it should be possible to reduce the number of gates.

4. Discussion

The simulation results have shown that the proposed polymorphic NAND/NOR gate and AND/OR gate controlled by Vdd can be used as standard building blocks for complex polymorphic circuits. In particular, it was confirmed that these polymorphic gates might be interconnected into circuits containing standard gates. Currently, these polymorphic circuits operate up to a few MHz. Their power consumption is reasonable. A next step is to validate the obtained results through a fabrication process.

Unfortunately, in order to offer useful polymorphic gates, we had to equip the original polymorphic gates with conventional inverters (i.e. with two transistors). These additional transistors represent a significant increase in the area on a chip in comparison with the original values reported in Table 1. Therefore, a new research is needed in the design of compact and efficient polymorphic gates.

Assume that we will be able to implement a reliable NAND/NOR gate using 6 transistors. As Table 2 shows a well-optimized solution containing 18 NAND/NOR gates and 5 AND gates exists for the four-input sorting network/two-bit multiplier circuit [7]. A conventional implementation of the four-bit sorting network requires 18 gates (9 ANDs, 9 ORs), i.e. 108 transistors (a standard CMOS AND as well as OR gate requires 6 transistors). The two-bit multiplier can be implemented using 7 gates (5 ANDs, 2 XORs), i.e. 50 transistors (XOR gate costs 10 transistors). Therefore, multiplexing the modules requires at least 158 transistors. Note that the cost of polymorphic multiplexers is not considered in this values and it is assumed that no gates can be reused in both modules. As the evolved four-input sorting network/two-bit multiplier circuit consists of 18 NAND/NOR gates and 5 AND gates, it costs 138 transistors, which represents a considerable reduction of the area on a chip in comparison with a potential solution based on polymorphic multiplexers.

The evolved three-bit multiplier/six-input sorting network is the most complex multifunctional circuit that has ever been evolved. The transistor-level simulations have confirmed that the utilized approach, in which firstly the circuit is evolved at the gate level and then is implemented at the transistor level, is a very promising way to the design of multifunctional modules. It seems that the evolutionary design of such complex circuits is impossible directly at the transistor level.

5. Conclusions

New nontrivial multifunctional circuits controlled by Vdd were proposed in this paper. Transistor-level simulations have confirmed their basic functionality. These circuits represent the most complex polymorphic circuits available nowadays whose behavior was validated at the transistor level. Next step is to validate these circuits on a real chip. In order to create more complex circuits, future research should primary deal with the design of robust polymorphic gates and the development of methodology for the design of multifunctional gate-level circuits. Simultaneously, it is desired to direct these research activities towards real applications.

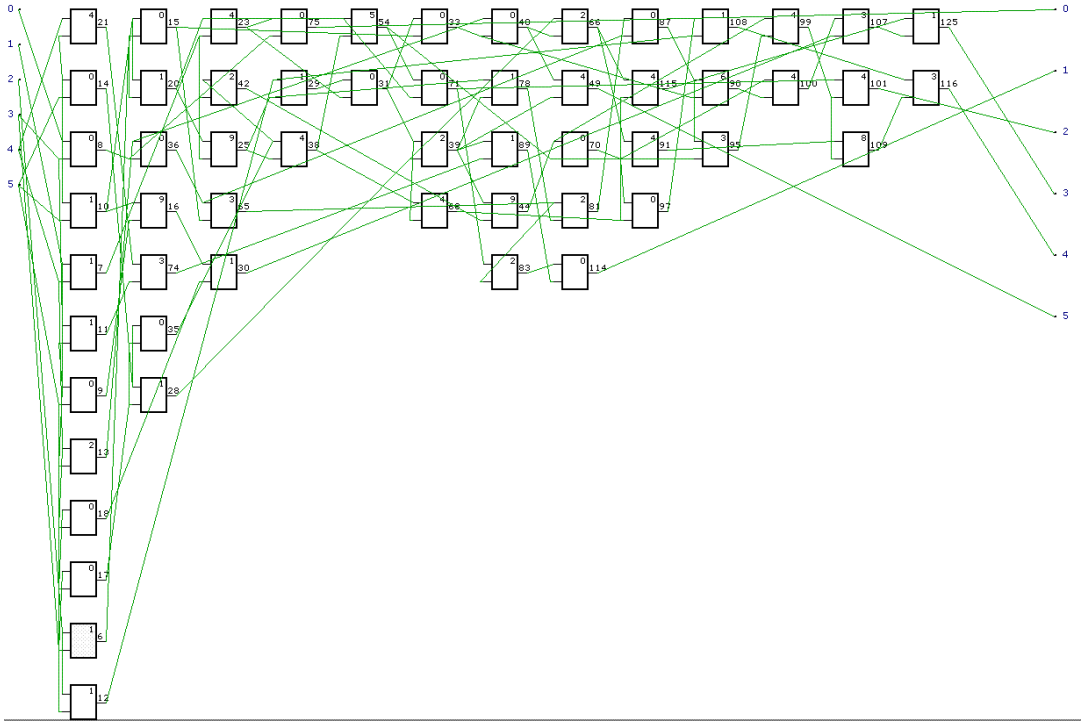

Figure 5. Evolved three-bit multiplier/six-input sorting network

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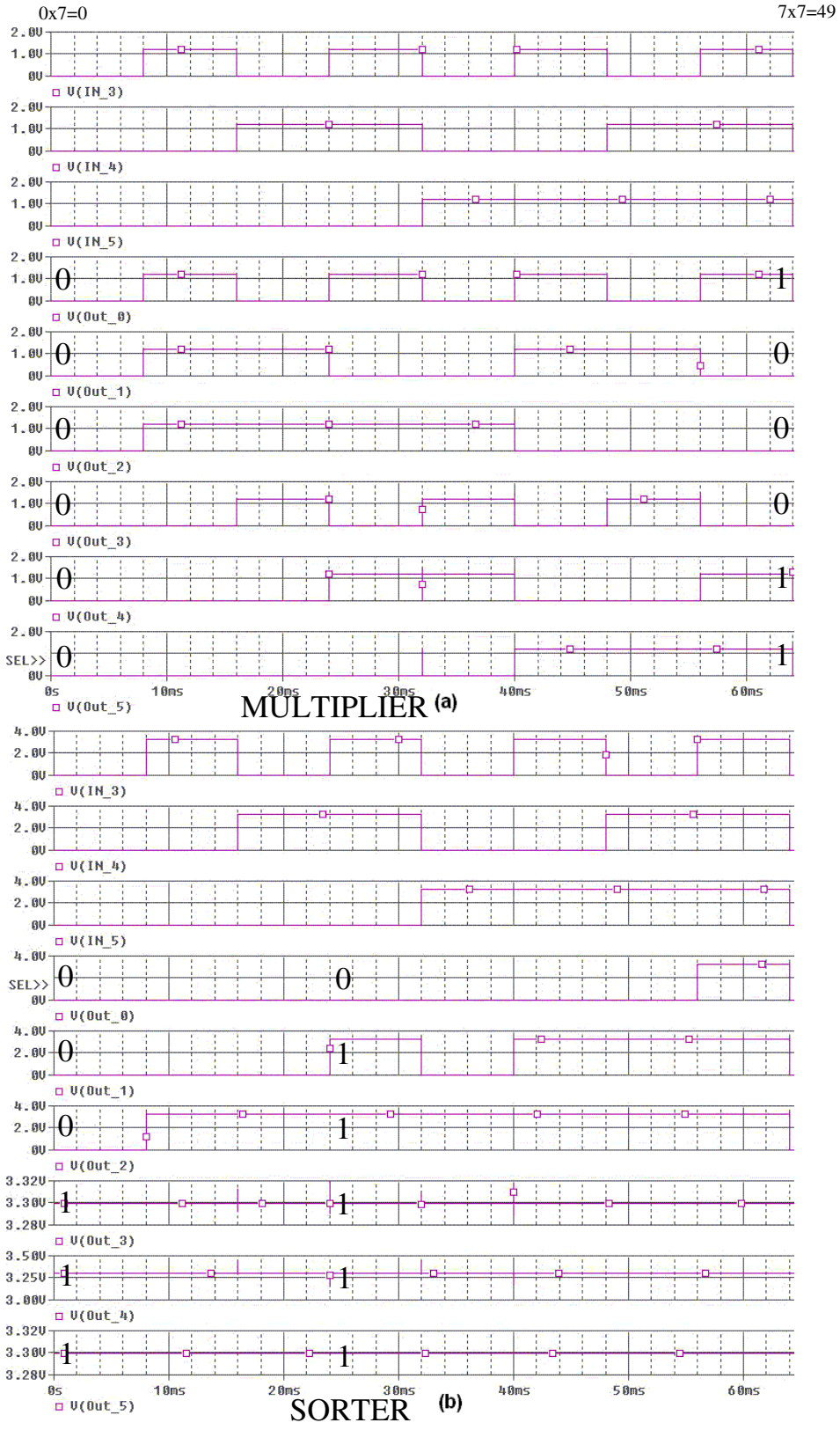

Figure 6. Simulation of three-bit multiplier/six-input sorting network: (a) multiplier for Vdd = 1.2V (b) sorting network for Vdd = 3.3V. The three lowest inputs are set at "111"