Educational Tool for the Demonstration of DFT Principles Based on Scan Methodologies

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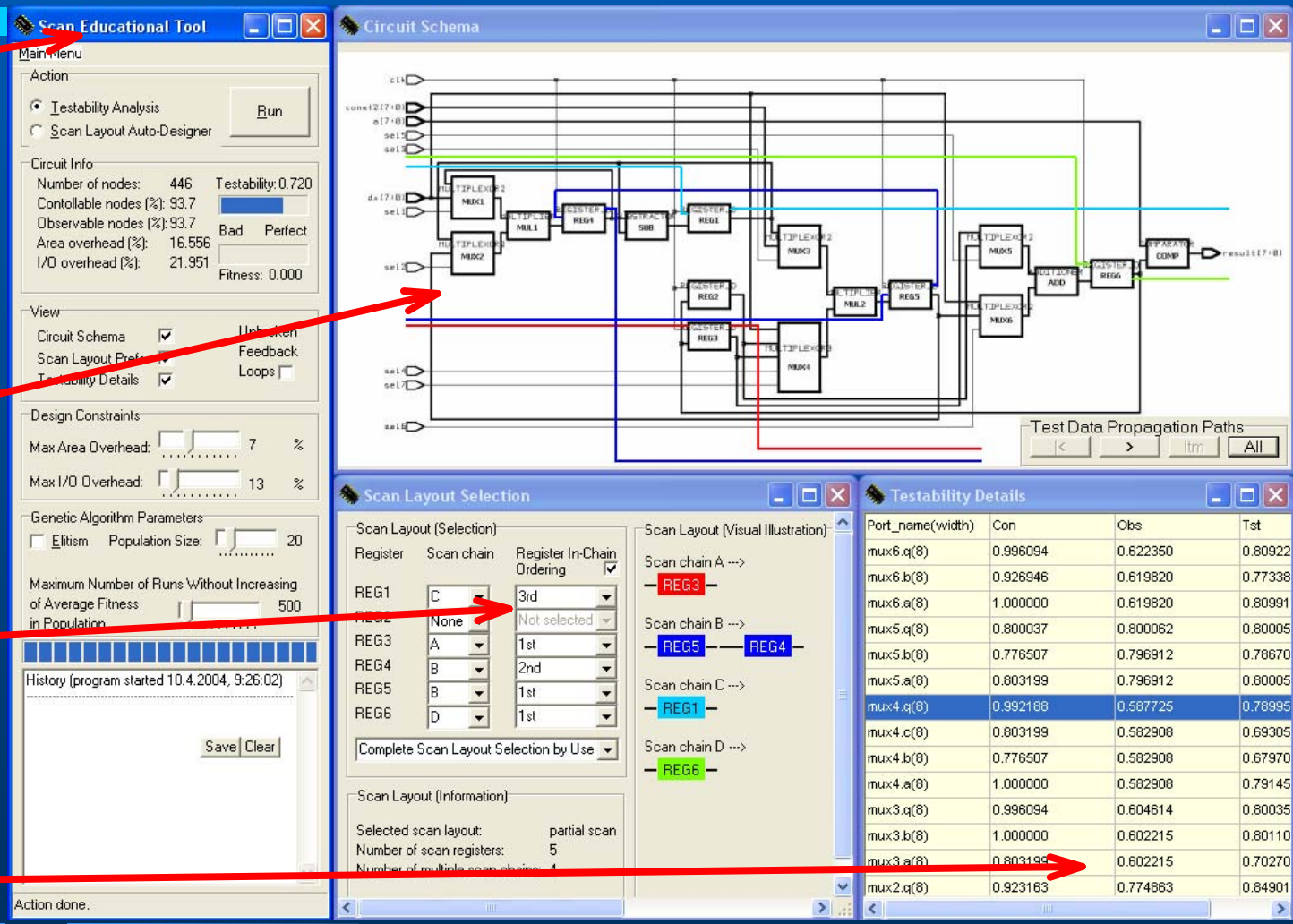
Presentation Outline

- Scan Educational Tool (SET)
- Description of particular SET windows
- Scan-layout selection example
- Testability analysis example
- Loop-breaking example
- Test data propagation paths browser example
- Automated DFT process example
- SET requirements and limitations
- Conclusions

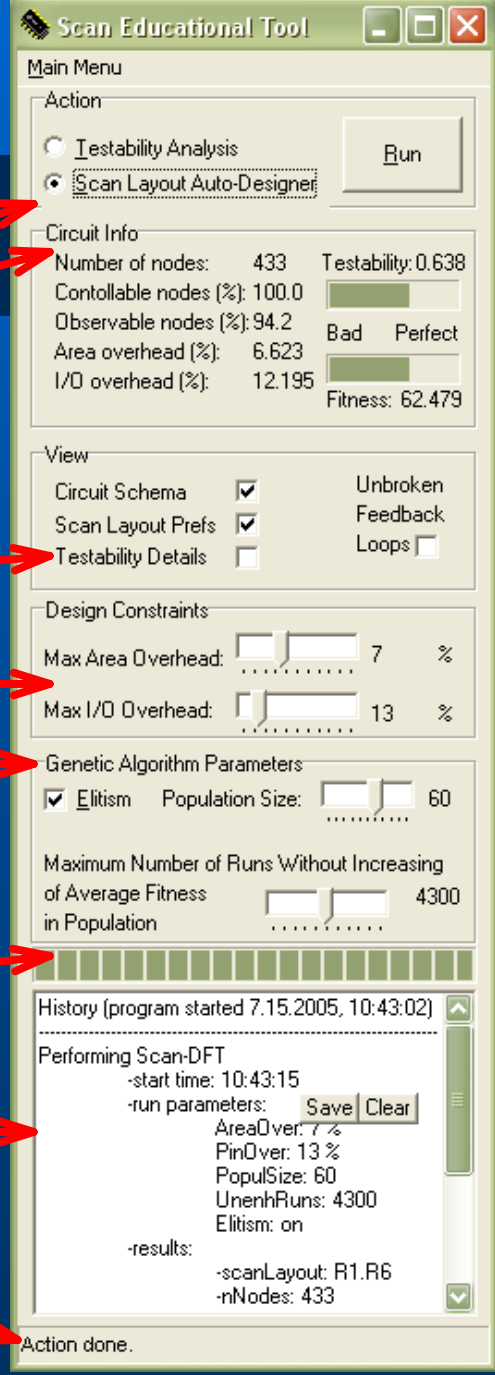
Scan Educational Tool (SET)

- **Main window**
  - TA/DFT selection
  - Circuit info
  - View selection
  - Design constraints settings
  - GA settings
  - History
- **Circuit schema**
  - Scan layout built in the circuit structure
  - Diagnostic data path browser
- **Layout selection**
  - Selection of registers into scan chains
  - Scan layout visualization
- **TA Results**

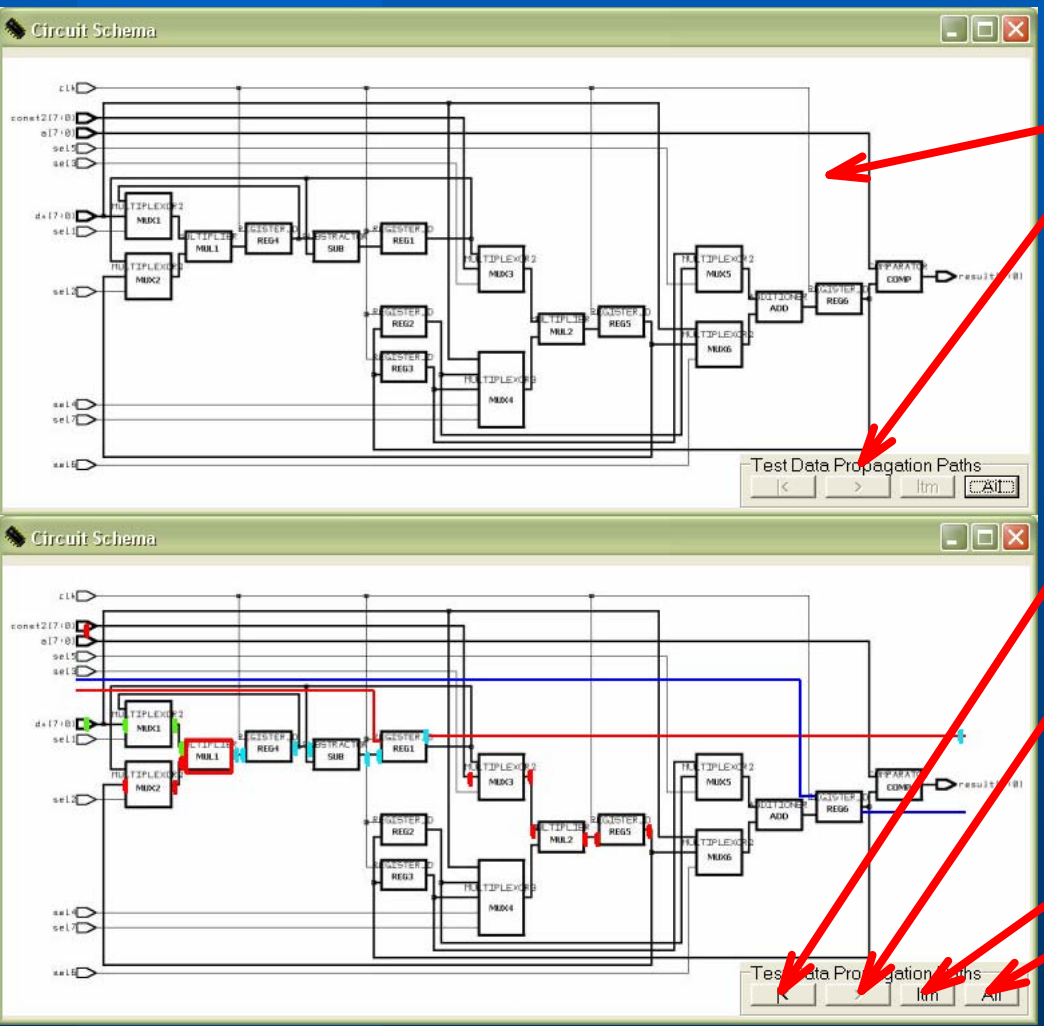


SET: Main window

- Action selection
- Circuit information (valid after action is done)
- Selection of windows to view
- Design constraints (area, I/O) settings
- Genetic algorithm settings
  - Elitism
  - Population size
  - Max # of runs
- Progress bar
- History (setting+result logging) window
- Status bar (current action info)



SET: Circuit schema window

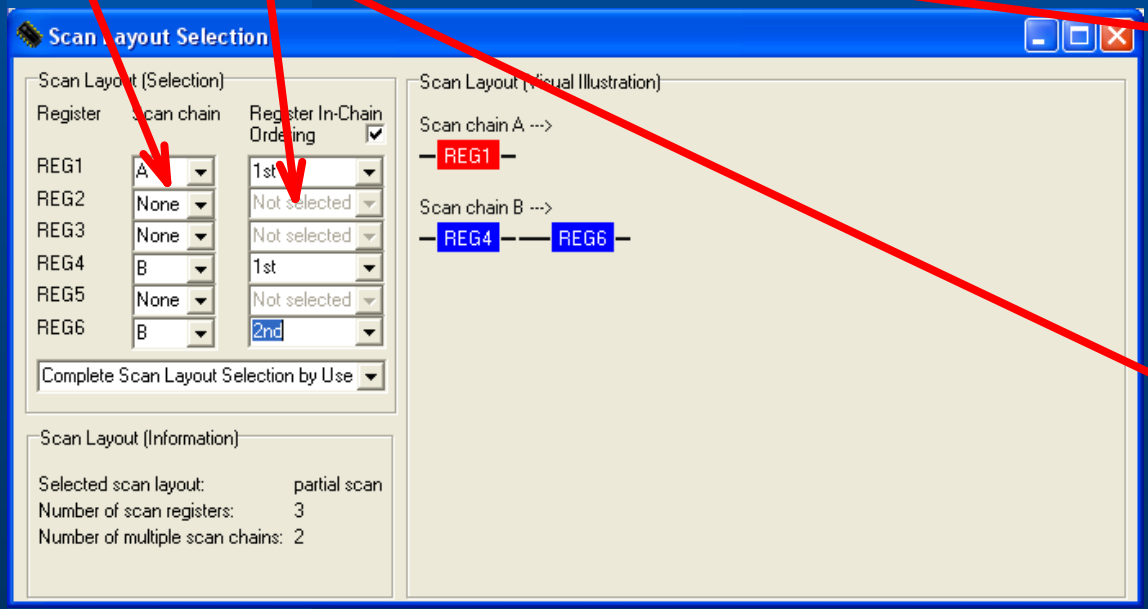


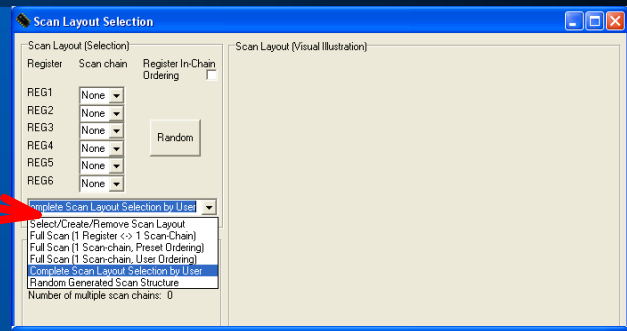
- Educational circuit schema
- Test data propagation paths browser for selected functional unit
  - Go to the path-start (primary inputs)
  - Perform 1 step towards path-end (primary outputs)
- Write information about test data propagation paths of
  - Selected functional unit
  - All functional units

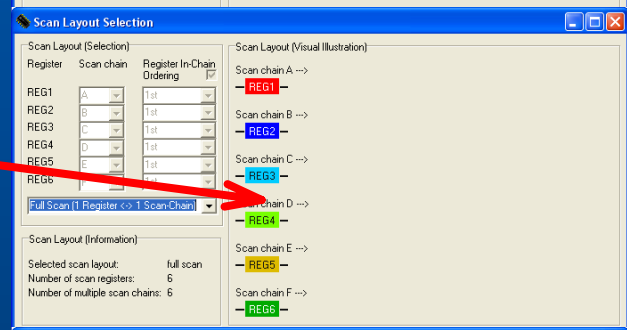
  into History window

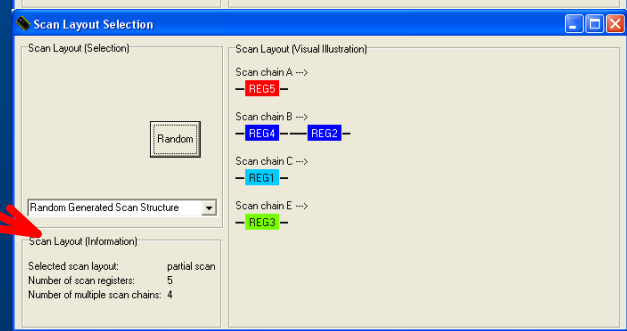
SET: Scan-layout window

- User/predefined/random (U/P/R) scan-layout selection
- U/P/R inclusion of registers into scan chains
- U/P/R ordering registers within scan chains
- Selected scan-layout
  - Vizualization
  - Information



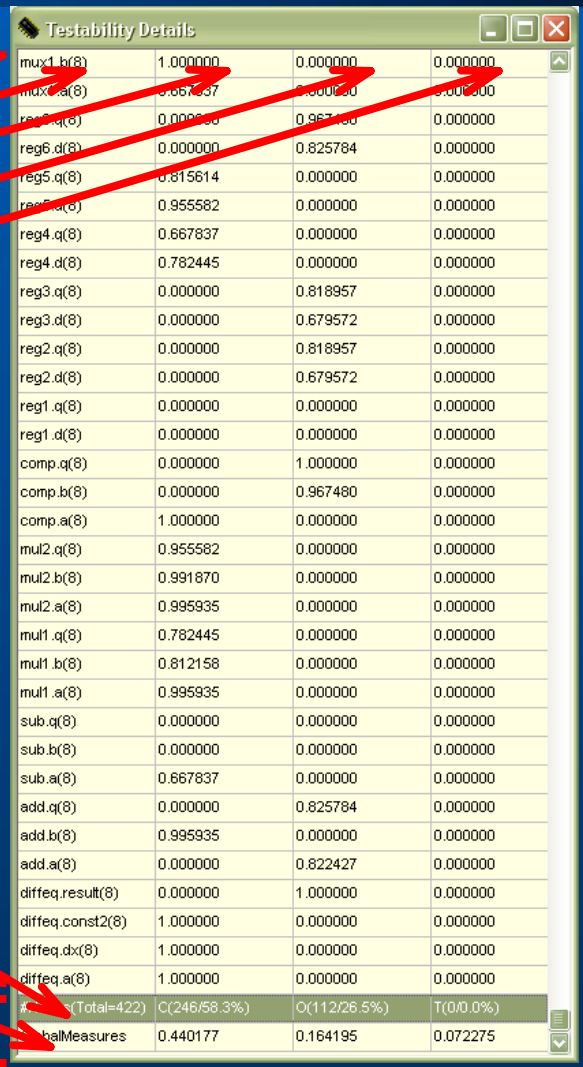




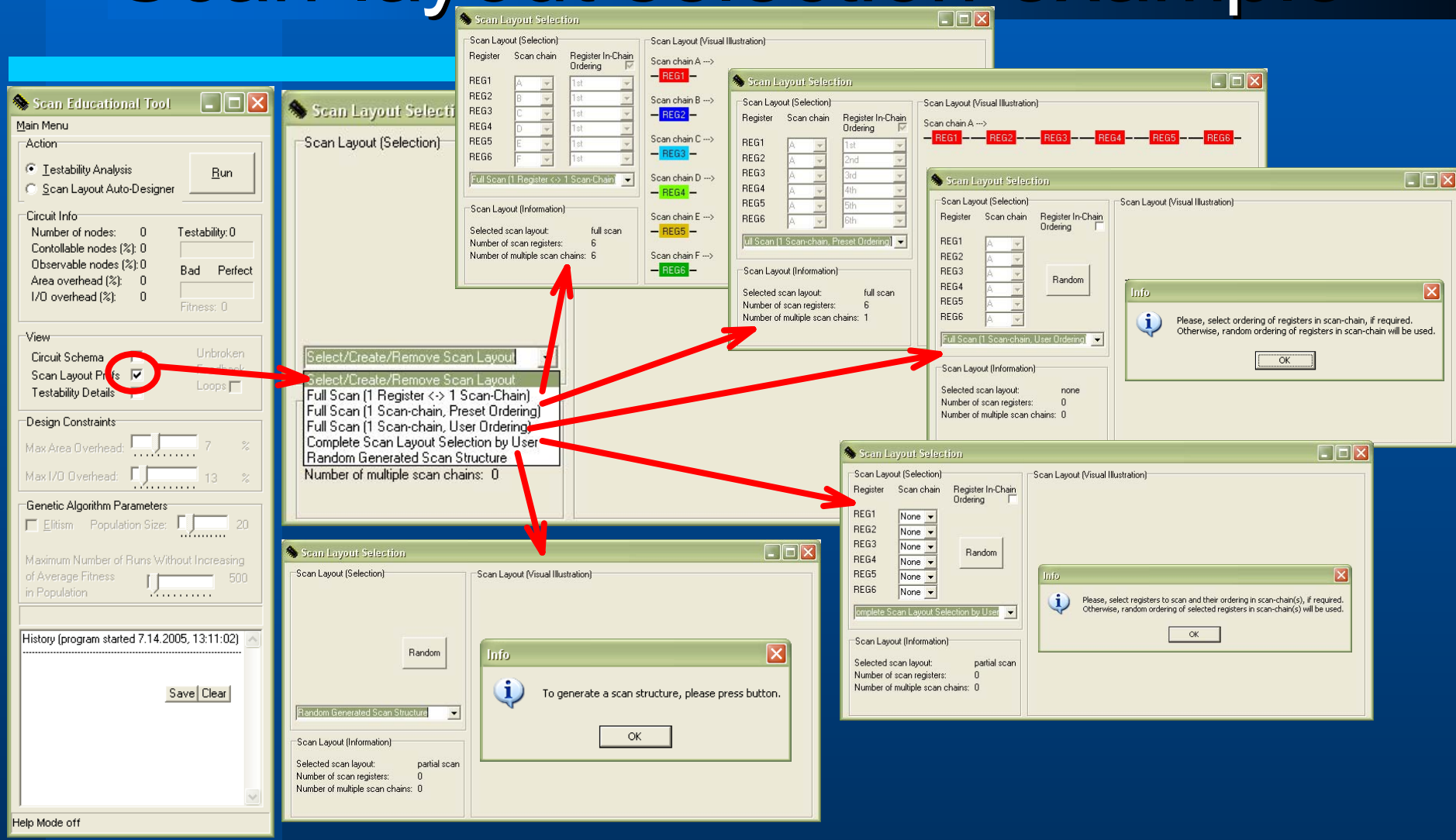


SET: Testability results window

- Port information
  - Name and bit-width
  - Controllability
  - Observability
  - Testability
- Summary information
  - "Nodes"
    - #/ratio of controllable nodes
    - #/ratio of observable nodes
    - #/ratio of testable nodes
  - "Circuit"
    - Controllability
    - Observability
    - Testability



Scan-layout selection example



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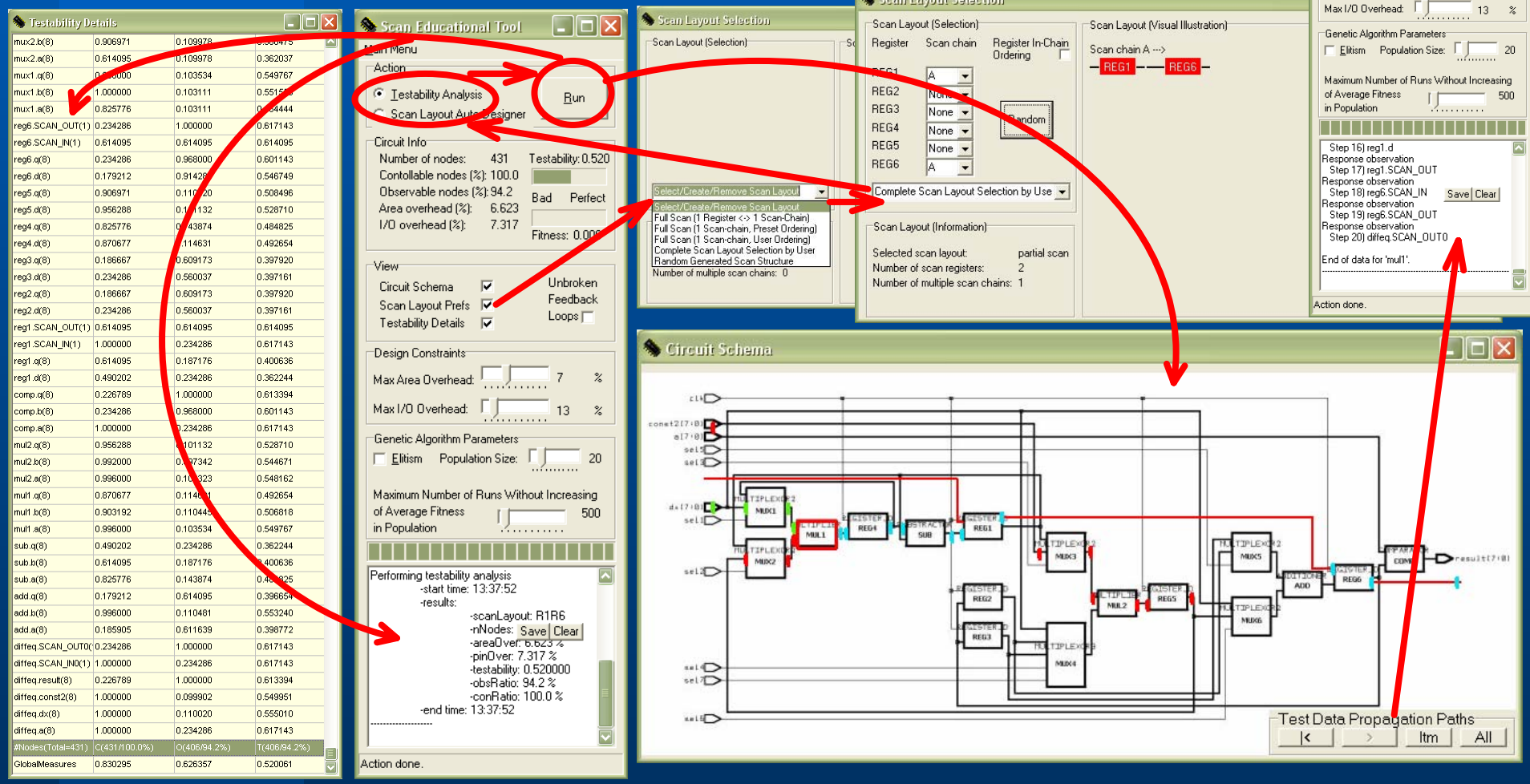
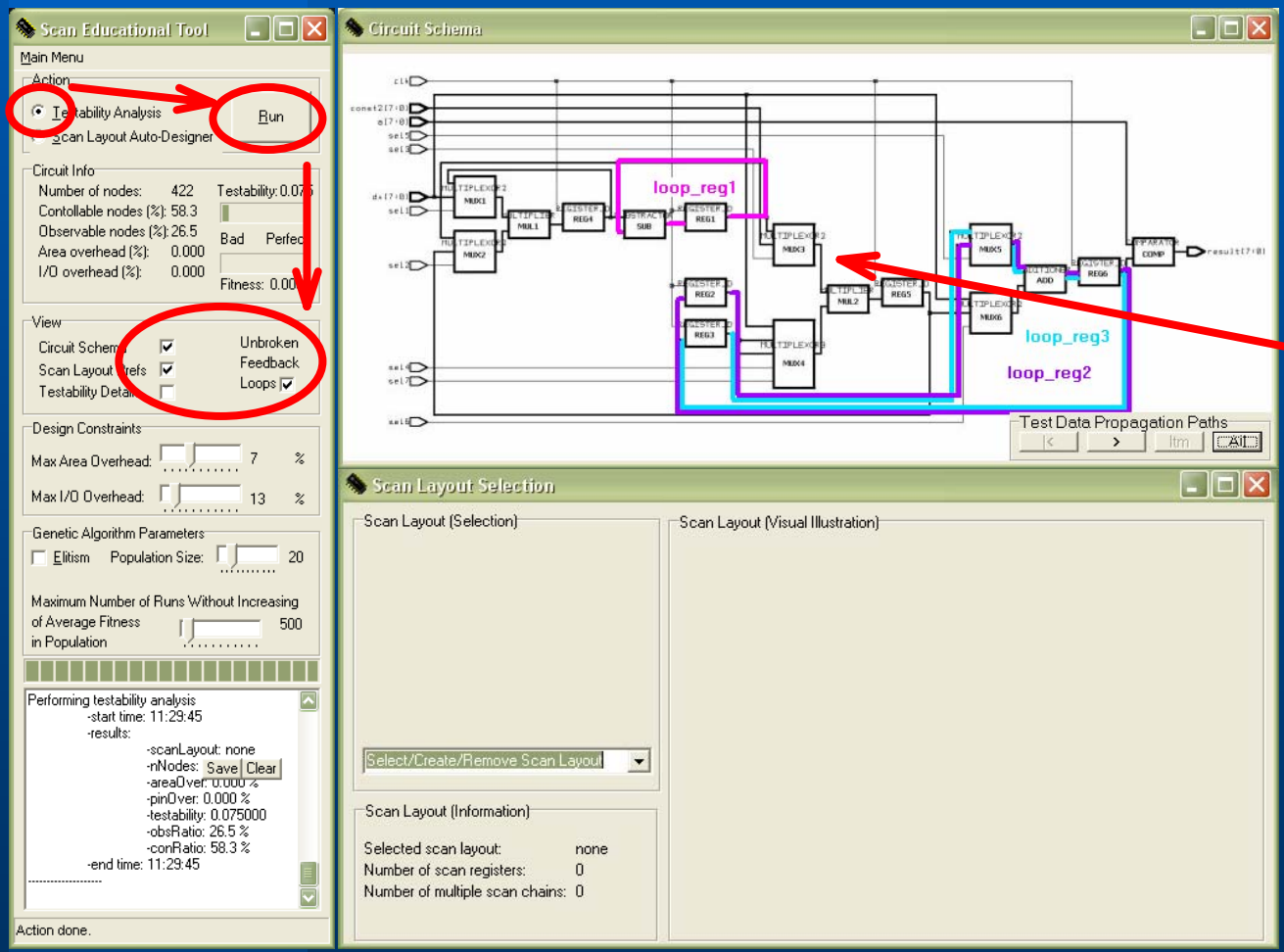
Testability analysis example



Loop-breaking example (1)

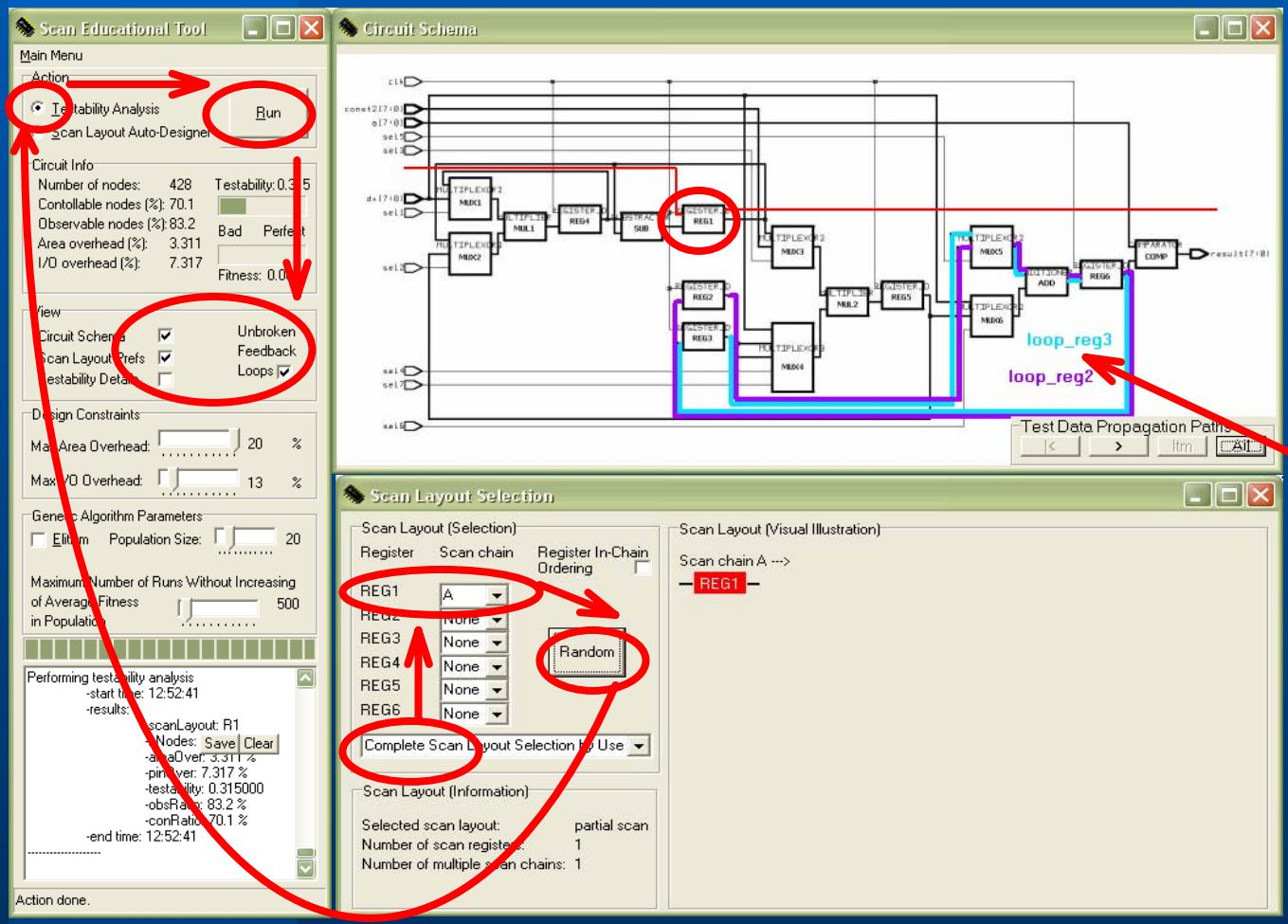


When
no scan-layout
is selected

then

all 3 loops
remain
unbroken

Loop-breaking example (2)

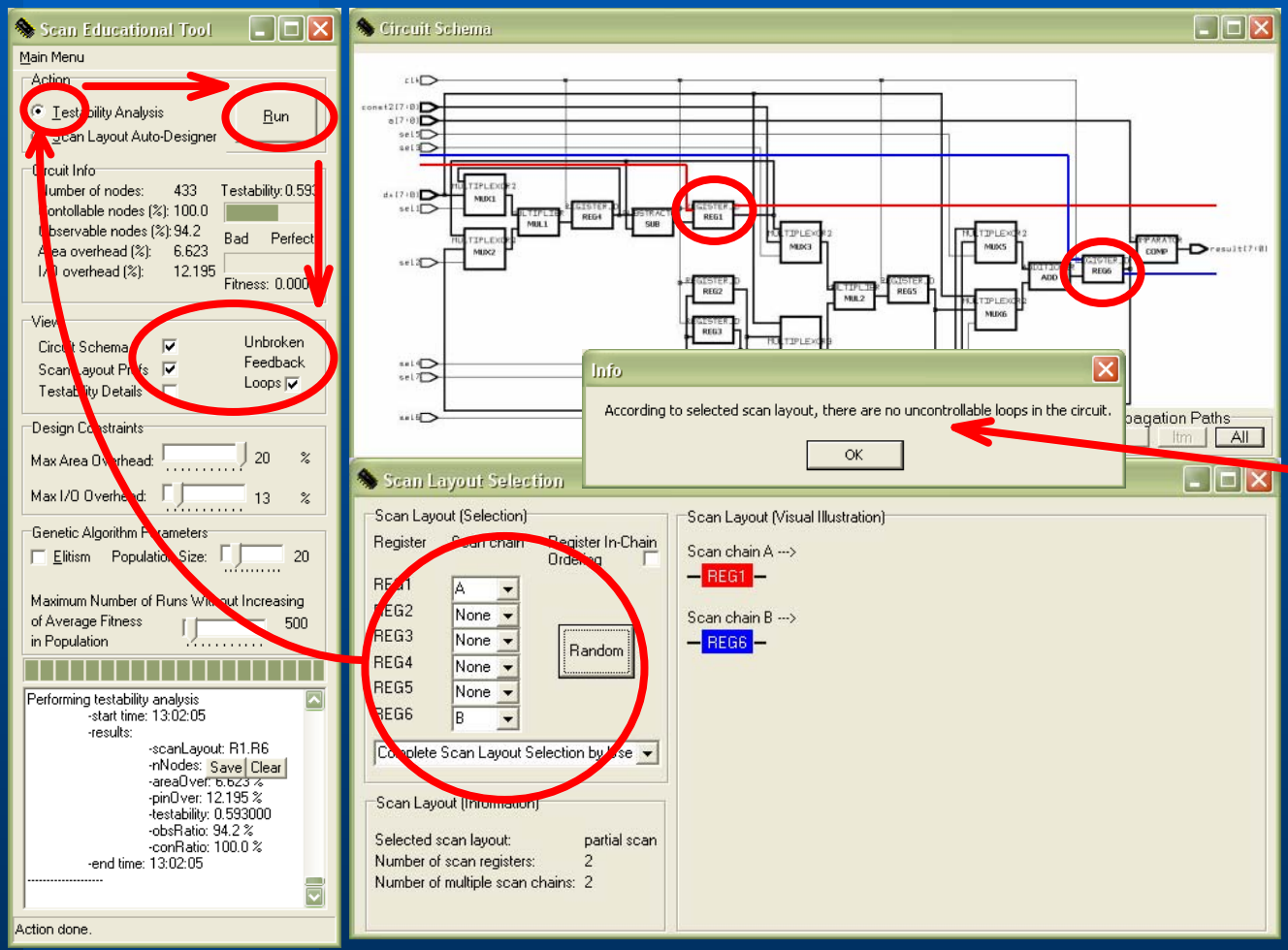


When REG1 is included into scan chain A

then

2 of 3 loops remain unbroken

Loop-breaking example (3)

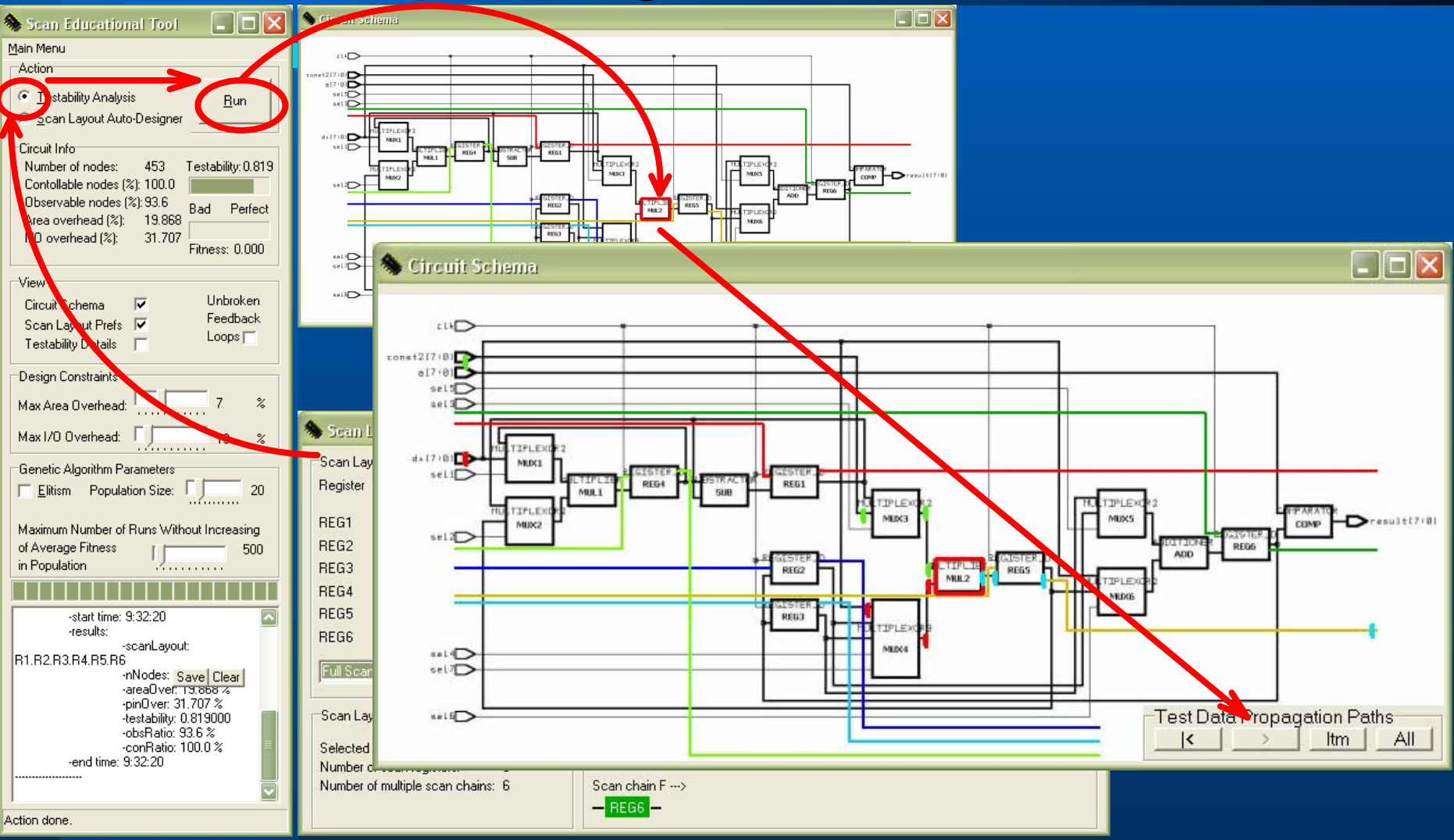


When REG1, REG6 are included into scan chains

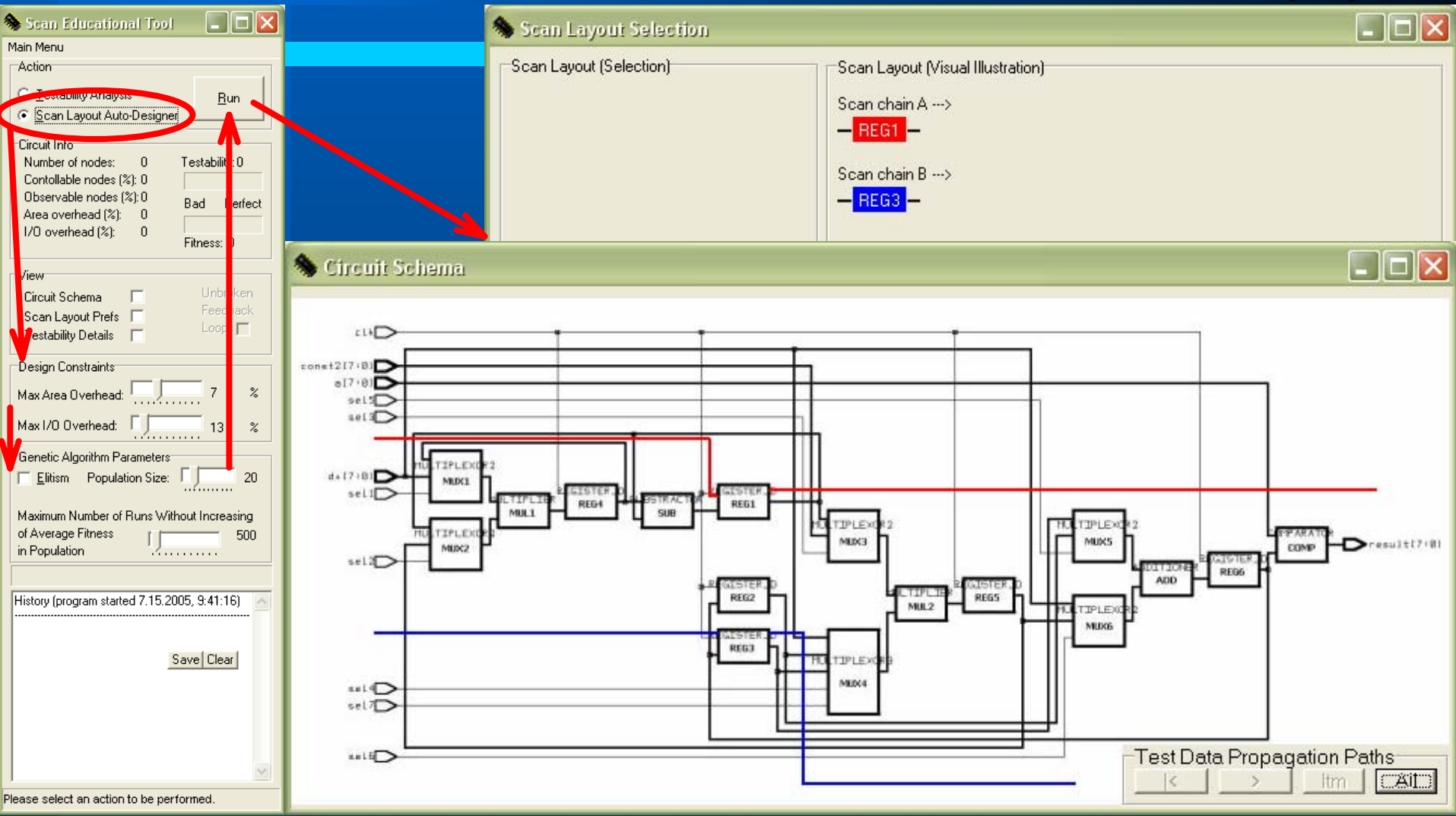
then

all 3 loops become broken

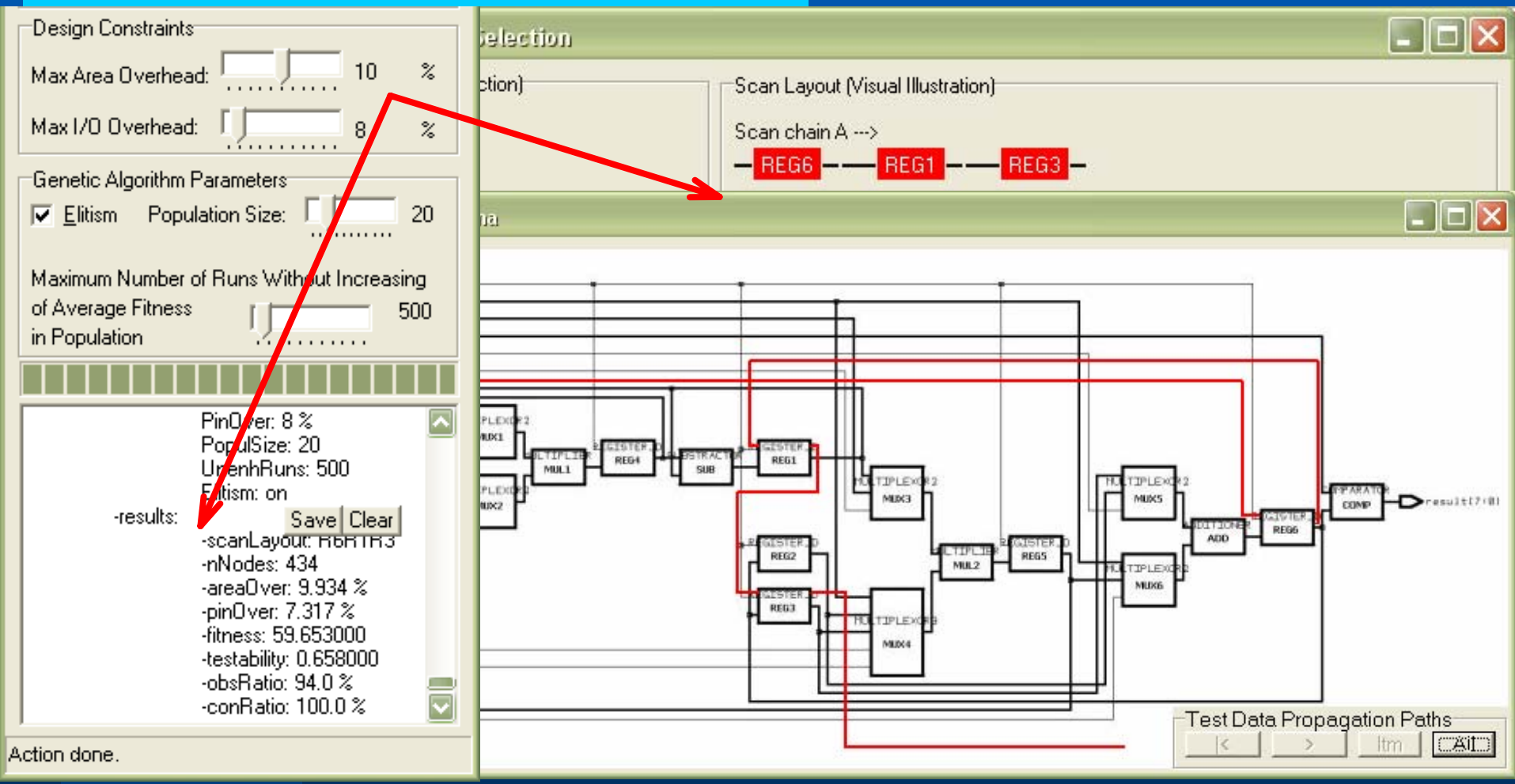
Test data propagation paths browser



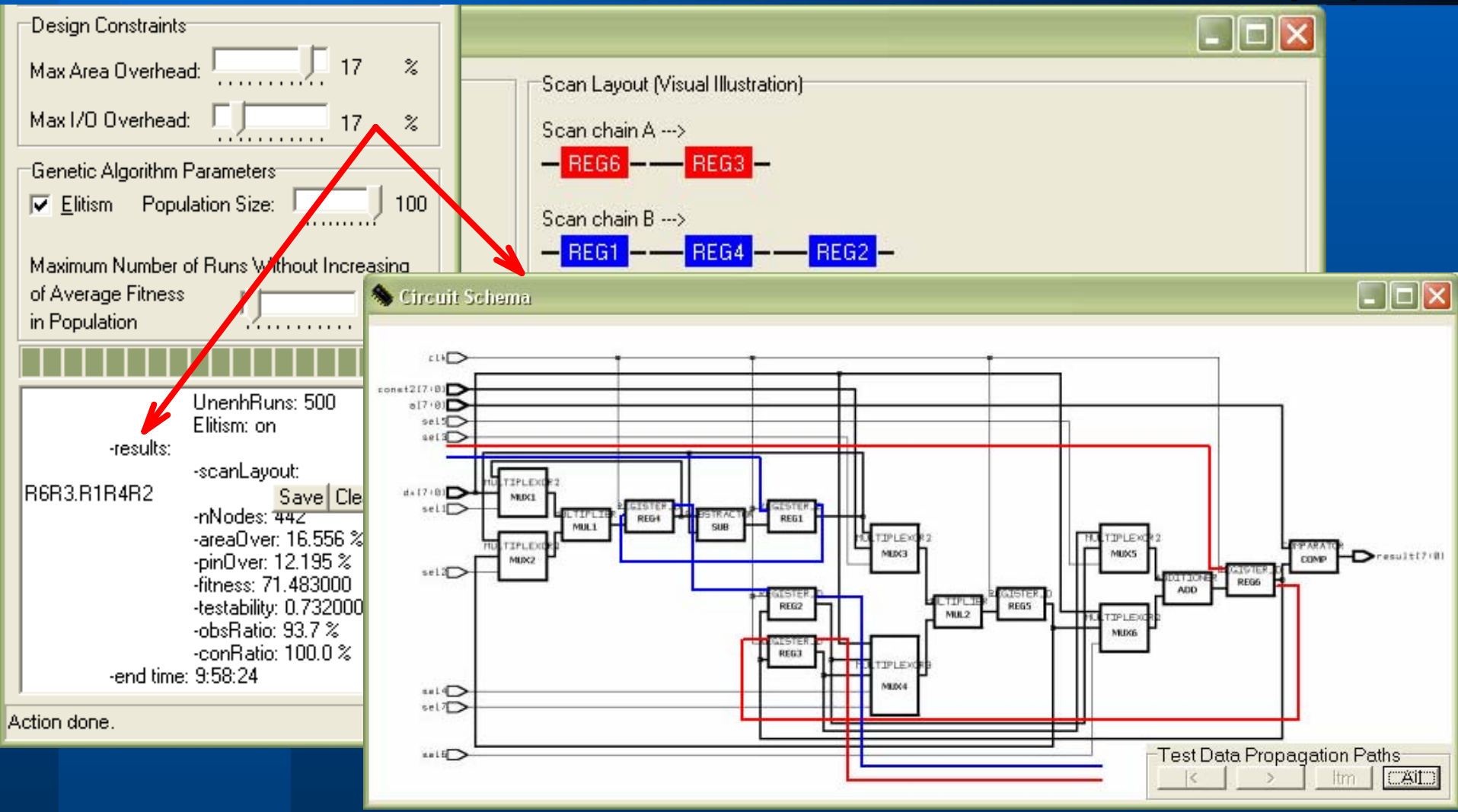
Automated DFT process example (1)



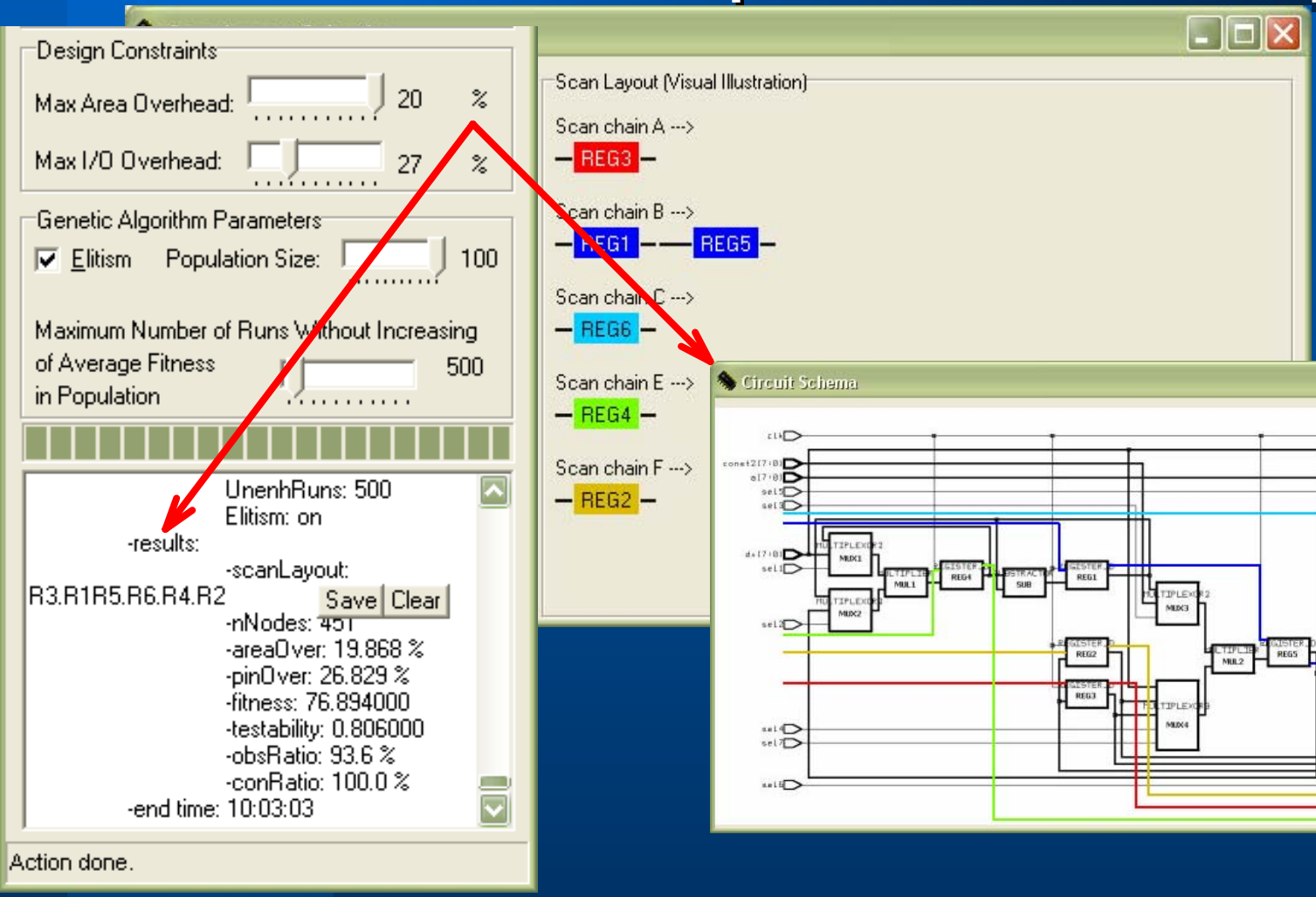
Automated DFT process example (2)



Automated DFT process example (3)



Automated DFT process example (4)



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SET requirements and limitations

Actual SET:

- **Requirements**
  - **WIN32 environment to run SET in graphical user interface mode**
  - **Original/emulated MS-DOS environment to run SET in command line mode**
- **Limitations**
  - **Non-commercial use only (see SET licencing conditions)**
  - **Set of educational circuits is limited to one circuit in the set**

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Conclusions

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