At-Speed Wiring Interconnects Testing on COMBO6 card

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Abstract.
In the paper an approach for at-speed board-level interconnection faults diagnosis of Combo6 card is presented. Existing methods and their limitations are briefly discussed first. Then, one-step diagnosis method for diagnosis of Combo6 wiring interconnects is presented. The method is based on utilization of "Universal Test Set" [3]. Designed method allows identification of static faults (with fault type determination) and detection of dynamic faults.

1 Introduction

The article deals with interconnection diagnosis of Combo6 card. Combo6 is a universal PCI card, which can be used in various applications. It consists of Xilinx Virtex II FPGA, 2Mb TCAM, 256MB DRAM and 6Mb SSRAM (see [4] for details). Various add-on cards can be used with Combo6 card. Add-on SFP card with 4 GE interfaces and 2 Virtex II FPGAs is an example of one of the Combo6 interface cards. The communication between interface and Combo6 card is realized via 100-bits wide 3-state bus with maximal clock frequency of 153MHz (maximal DDR transfer rate is approx. 3,8GB/s). Unfortunately the interconnection connector between Combo6 and its interface card is often source of reliability problems. Therefore, it bacame a must to deal with task of implementing at-speed diagnosis of the interconnection system.

2 Algorithms for Wiring Interconnection Test

Interconnection test is in most cases realized so that a unique code word (sequential test vector – *STV* [2]) is assigned to each net. If the nets are fault-free, each response (sequential response vector – *SRV*) is unique. When there is a short, the nets involved have the same response. Therefore, these responses are no longer unique and the test detects the short. Many algorithms for interconnection testing exist nowadays (e.g. Modified Counting Sequence algorithm, LaMa algorithm, True/Complement algorithm, ...). Fault detection is guaranteed by most of interconnection test algorithms, but diagnostic resolution of a test is another important property. In [2] *aliasing* and

confounding problems which affect test diagnostic resolution are introduced. *Aliasing* occurs when the faulty response of a faulty net is equal to the fault-free response of another, fault-free net. In this case, we cannot determine whether the fault-free net also suffers from the fault at the faulty net. *Confounding* problem occurs if the responses from multiple independent faults are identical. Therefore it cannot be determined if these faults are independent. Lien et al present an "Universal Test Set" [3] which solve both *aliasing* and *confounding* problem. The test set is based on walking-0 (provide maximal diagnosis when assuming wired-OR model of shorts and that floating net is modelled as a soft stuck-at one), walking-1 (assuming wired-AND model and that floating net is modelled as soft stuck-at zero) and all-0/1 test vectors are used to distinguish between the cases of all-nets are shorted and all-nets are open (see [3] for details). For k nets, it requires $2(k+1)$ test patterns. Example of matrix with test vectors for a network consists of 3 nets shows Equation 1. Rows of the matrix forms sequential test vectors and columns forms parallel test vectors. Each STV contains both transitions $0 \rightarrow 1$ and $1 \rightarrow 0$ which enables detection of delay faults.

$$S_{universal} = \left[\begin{array}{c|ccc|c|ccc} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 0 & 0 \end{array}\right] \quad (1)$$

3 Combo6 interconnection test

For Combo6 interconnection testing an algorithm based on "Universal Test set" was chosen because of its diagnostic properties. A TPG that can be used for at-speed testing at the frequency of 153MHz (306MHz for DDR transfer) was needed. A TPG based on modified LFSR register was developed (Figure 2). N-bit TPG consists of $(n+2)$ D flip-flops and XOR gates. The first $(n+1)$ D flip-flops are interconnected in the following manner: each input of nth D flip-flop is connected to the XOR gate which behaves as a controlled inverter and output of the gate is connected to the input of $(n+1)$th D flip-flop. The last $(n+2)$th D flip-flop is used for controlling XOR invertors between the first $(n+1)$ gates. The maximal frequency of the TPG is 333.6MHz (Leonardo Spectrum time analysis of implementation on Virtex II v3000). Thus, the TPG can be utilized to implement Combo6 interconnection diagnosis.

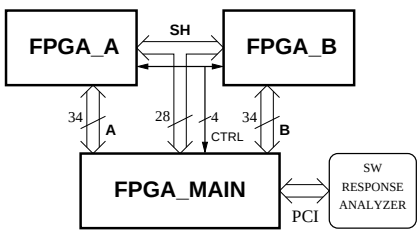

Figure 1: The FPGAs interconnection diagram

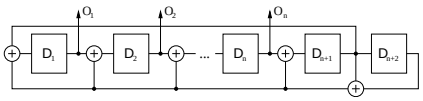

Figure 2: Test pattern generator

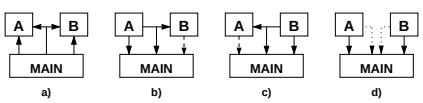

Figure 3: Test schema

The diagnosis was implemented as one-step diagnosis. All test vectors are applied to tested nets and responses are evaluated by the software. The diagram of FPGAs interconnection system is shown in Figure 1. It can be seen that three FPGAs are interconnected mutually with 3-state nets. Each FPGA on interface card is connected

directly to FPGA on Combo6 card with 34-bits nets (A, B) and all FPGAs are connected to the shared 32-bits bus (SH). For purposes of interconnection test four nets of the shared bus are used for control signals. Testing of these four nets can be performed by design with similar source code – only modification of *User Constraints File* is needed.

Interconnection test is performed in four steps (see Figure 3). In the first step $FPGA_{MAIN}$ is active as TPG – 96 bits test vectors are applied to A, B and SH nets and two Virtex II BlockRAMs in each $FPGA_A$ and $FPGA_B$ are used to store response vectors. In the second step $FPGA_A$ is active as TPG – 62 bits test vectors are applied to nets. In this step, the $FPGA_B$ is used to transfer response vectors from its SH input to B output (vectors on B output will be one clock delayed) and $FPGA_{MAIN}$ stores 96 bits response vectors to BlockRAMs. The third step is analogous to the second step, but $FPGA_B$ is active as TPG. In the fourth step $FPGA_A$ and $FPGA_B$ use A and B connections to transfer response data from FPGAs BlockRAMs on interface card to $FPGA_{MAIN}$. SH bus is not used, but it can be used for example for transfer parity bits for data transported through A and B connections.

Diagnostic data are transferred via PCI bus to SW response analyzer (implemented in C++) and results of interconnects diagnosis are written out.

4 Conclusions

In the paper, the approach utilized for at-speed wiring interconnection testing on Combo6 card was presented. The approach is based on utilization of the "Universal Test Set". A TPG generating the required test sequence was developed and used. The developed TPG is able to generate parallel test vectors at approx. 300MHz speed. The utilized approach based on this TPG allows one-step diagnosis with identification of static and dynamic faults to be performed. It can be stated that other approaches for interconnection testing with less time complexity exist but these algorithms work in more steps or have worse diagnostics properties.

Acknowledgements

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